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Multilevel multistate hybrid voltage regulator

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Multilevel Multistate Hybrid Voltage Regulator

A thesis submitted in partial fulfillment of the requirements
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A thesis submitted by:

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Dedicated to My Parents. For Their Endless Love, Support and Encouragement . . .

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Abstract

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Multilevel Multistate Hybrid Voltage Regulator

by Abdallah Amgad

In this work, a new set of voltage regulators as well as some controlling methods and schemes are proposed. While normal switched capacitor voltage regulators are easy integrable, they are suffering from charge sharing losses as well as fast degradation of efficiency when deviating from target operation point. On the other hand, conventional buck converters use bulky magnetic components that introduce challenges to integrate them on chip. The new set of voltage regulators covers the gap between inductor-based and capacitor-based voltage regulators by taking the advantages of both of them while avoiding or minimizing their disadvantages.

The voltage regulator device consists of a switched capacitor circuit that is periodically switching its output between different voltage levels followed by a low pass filter to give a regulated output voltage. The voltage regulator is capable of converting an input voltage to a wide range of output voltage with a high efficiency that is roughly constant over the whole operation range. By switching between adjacent voltage levels, the voltage drop on the inductor is limited allowing for the use of smaller inductor sizes while maintaining the same performance. The general concept of the proposed voltage regulator as well as some operating conditions and techniques are explained.

A phase interleaving technique to operate the multilevel multistate voltage regulator has been proposed. In this technique, the phases of two or more voltage levels are interleaved which enhances the effective switching frequency of the charge transferring components. This results in a further boost in the proposed regulator's performance.

A 4-level 4-state hybrid voltage regulator has been introduced as an application on the proposed concepts and techniques. It shows better performance compared to both integrated inductor-based and capacitor-based voltage regulators. The results prove that the proposed set of voltage regulators offers a potential move towards easing the integration of voltage regulators on chip with a performance that approaches that of off-chip voltage regulators.

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Abbreviations

VR	**V**oltage **R**egulator
MMVR	**M**ultilevel **M**ultistate **V**oltage **R**egulator
PIT	**P**hase **I**nterleaving **T**echnique
SC	**S**witched **C**apacitor
SCC	**S**witched **C**apacitor **C**ircuit
SCVR	**S**witched **C**apacitor **V**oltage **R**egulator
LPF	**L**ow **P**ass **F**ilter
DVFS	**D**ynamic **V**oltage and **F**requency **S**caling
PWM	**P**ulse **W**idth **M**odulation
DPWM	**D**igital **P**ulse **W**idth **M**odulator
CCM	**C**ontinous **C**onduction **M**ode
DCM	**D**iscontinous **C**onduction **M**ode
KVL	**K**irchhoff's **V**oltage **L**aw
MOSFET	**M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor
RMS	**R**oot **M**ean **S**quare
AC	**A**lternating **C**urrent
DC	**D**irect **C**urrent

Chapter 1

Introduction

1.1 Motivation

The IC technology is scaling down allowing for more circuits to be integrated on one chip. Current progress in integrated circuits drives the continuing development of power management, conversion and regulation techniques. Power management techniques have been developed to help managing the power consumption of the increasing number of components on the chip. The existence of low power circuits, high speed digital circuits, and analog circuits on one chip (i.e. system on chip SoCs) drives the need for several supply voltages on one chip. Providing this high number of supply voltages from outside the chip requires larger number of I/O pins which requires additional packaging cost and area. Moreover, the number of I/O pins per chip is limited especially that large number of them would be used as power pins to handle these several supply voltages. Furthermore, the reduced size of portable electronics limit the use of external bulky components required to generate and decouple these multiple voltage supplies. Full integration of voltage regulators on chip not only helps in overcoming packaging and external complexity but also introduces additional internal benefits on the chip. First,

integrated voltage regulators decouples the internal circuits from the pad and packaging parasitics that cause large swings in supply voltage [1]. Second, multiple supply voltages can be generated on chip using only one external supply saving a considerable number of I/O pins. Third, each single supply voltage can be controlled independently to automatically adapt to changes in the environment and load conditions of that circuit [2]. Finally, delivering the total external power to the chip at high voltage then scaling down this voltage locally on chip would help in saving some overhead area and circuitry associated with power delivery network in a manner similar to AC power distribution systems.

The trend nowadays is to lower the power consumption of ICs especially for battery-operated devices. The active and sleep power consumption can be reduced by using Dynamic Voltage and Frequency Scaling (DVFS) [3] and body-bias techniques [4]. In DVFS, circuits are partitioned into independent voltage islands [5] where each island operates at its own supply voltage. This supply voltage level can go up or down according to the desired performance from this island. This helps in saving the total power consumption of the circuit but requires a separate voltage regulator for each island to provide its supply voltage level. The body-bias techniques can be used to control the threshold voltage of transistors and hence control their leakage current especially in sleep mode. In active mode, a forward body bias is applied to increase the speed of digital circuits by decreasing the threshold voltage of transistors.

Today's modern high performance processors have many cores integrated on one chip as shown in figure []. Each core is preferred to operate at its separate voltage domain to support the DVFS feature. This means each core requires a separate voltage regulator that has high efficiency over a wide range of output voltage levels [6]. Moreover, studies on processor workloads show large fluctuations in their activities in tight timescales that cannot be tracked by conventional coarse-grained DVFS techniques [7]. Fine-grained high-speed DVFS techniques where fast transitions in voltage level occur according to processing workloads would greatly

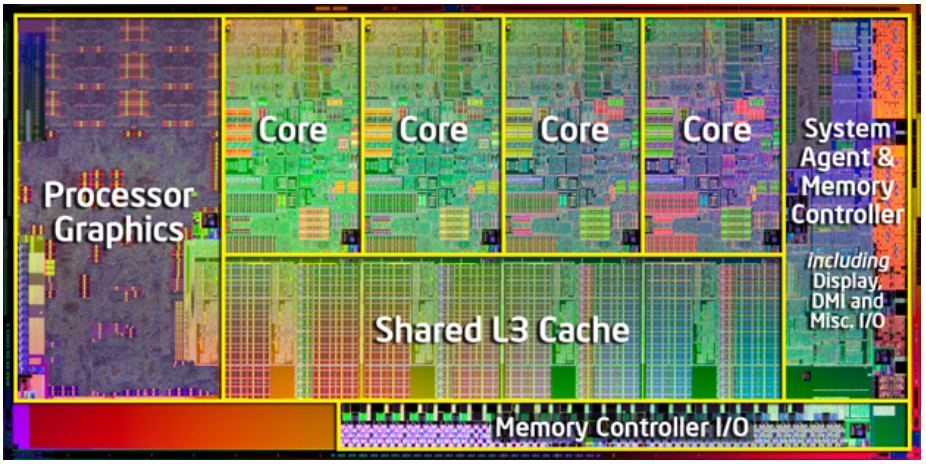


FIGURE 1.1: Intel Sandy Bridge Core i7 die map [8]

help in enhancing the core energy utilization. While off-chip voltage regulators uses bulky components and are operating at lower switching frequency which limits their voltage transition times, integrated voltage regulators offer opportunities to achieve such fine-grained DVFS feature as they are operating at much higher switching efficiency.

To sum up, efficient power management requires the control of the power consumption of each block separately. This exposes the need to integrate voltage regulators on chip which is an essential step for modern integrated circuits and is of high demand nowadays. That is what makes it a hot research area at present. This research trend is motivated by the benefits gained from integrating voltage regulators on chip. Despite the progress made towards that goal, many challenges are still ahead to have an efficient integration of voltage regulators on chip that satisfies the requirements of modern ICs.

1.2 Challenges and Requirements

There are two main existing ways to convert one voltage level into another. The first approach is by using linear regulators (i.e. continuous-time regulator) where

the conversion from input voltage to output voltage is done by a voltage drop on a resistance which is a dissipative element. In this case, only a step-down conversion is possible. The second approach is by using switch-mode voltage regulators where the required voltage difference between input and output voltage is provided by energy-storage elements like inductors and capacitors. In this case, step-up and/or step-down conversions are available.

The linear regulators [9, 10], conventionally known as Low Dropout regulators (LDOs), are efficient when desired output voltage (V_o) is near input voltage (V_{in}). This is mainly because their maximum efficiency is always given by V_o/V_{in}. Once the difference between V_{in} and V_o is large, the efficiency degrades substantially where most of power are dissipated in the resistance that provides the voltage drop. Therefore, LDO regulators lack the support for DVFS feature which is a very important feature for modern ICs as discussed previously. This is considered a fundamental limit of LDO regulators. On the other hand, switch-mode voltage regulators offer the potential to support large voltage conversion difference with efficiency higher than that of LDO regulators. Consequently, they are gaining more attention nowadays.

Unlike linear regulators, there are many challenges when it comes to integrating switch-mode voltage regulators on chip. This is because they depend on bulky storage elements that when integrated on-chip are of smaller sizes and worse quality factors than their off-chip counterparts. Although integrated voltage regulators are usually of worse performance than their off-chip counterparts, the advantages that can be gained from integrated voltage regulators drive the motivation to continue in this way. The goal is to have on-chip voltage regulators with a performance that is comparable with that of off-chip regulators.

The requirements from modern integrated voltage regulator can be summarized as follows:

- Full or wide access to the whole range of input voltage.

- High efficiency over wide range of operating points (output voltages and load currents).
- Low output voltage ripples over the whole operation range.
- Fast transient response to changes in load current and reference voltage.
- Easy integrable on-chip with less bulky components which means small or no magnetic components.
- Higher power density so the area cost is reduced.

Although there are promising paths to achieve these requirements, there are a lot of challenges still exist ahead that need to be addressed. These challenges are well illustrated in the next chapter where an analysis study on both main types of switch-mode voltage regulators is provided.

1.3 Organization of Thesis

The goal of this work is to introduce a new set of voltage regulators that offer solutions to current challenges facing integrated voltage regulators.

Chapter 1 provides a literature review on the two main types of switch-mode voltage regulators where the limitations of each type are discussed. It comes up with a conclusion that a hybrid structure may offer an optimum solution to integrated voltage regulators.

The proposed multilevel multistate voltage regulator (MMVR) is introduced in chapter 2. Its general structure and operation principle along with some operating conditions are explained in detail. After that, a comparison with inductor-based and capacitor-based voltage regulators is done proving that the MMVR offers significant performance improvements over the other two types.

A phase interleaving technique (PIT) to operate the MMVR is proposed in chapter 3, offering a further boost in MMVR performance. Some analysis on the effect of phase interleaving technique on circuit performance is provided where the effective switching frequency of each component in MMVR is investigated.

A 4-level 4-state voltage regulator is proposed in chapter 4 as a design implementation based on MMVR general structure and principles mentioned in chapters 2 and 3. The circuit structure and operation are discussed along with a comparative analysis to other two main types of voltage regulators. Two implementations of the circuit on two different CMOS technologies are done. Simulation results show that the 4-level 4-state VR offers the highest performance compared to existing literature work.

Finally, a conclusion, provided in chapter 5, comes out that the MMVR is a general structure for VR offering potential solutions to modern challenges in VRs. Many implementations based on these concepts and techniques can be done as a future work along with more analysis to get a deeper insight into the MMVR.

Chapter 2

Background and Literature Review

2.1 Introduction

Any voltage regulator circuit consists of a combination of charge transferring components which are switches, capacitors and inductors. Since capacitors and inductors are charge storage elements, staying at one state only would cause them to saturate at a certain limit and in this case no charge transferring occurs. Therefore, a charging/discharging process has to be performed by switching between different phases. Hence, they are called switch-mode voltage regulators. Depending on the type of the main component used to transfer charges between input and output, there are two types of switch-mode voltage regulators: Inductor-based voltage regulators and capacitor-based voltage regulators.

In this chapter, a quick overview of both main types of switch-mode voltage regulators is presented. First, their working principle is briefly explained. After that, the main limiting factors of each voltage regulator type are investigated along with trials in the literature work to overcome these limitations. This chapter is

ended by a conclusion that leads to the next chapter introducing the proposed multilevel multistate voltage regulator.

2.2 Voltage Regulator Metrics

There are some general metrics used to evaluate different types or topologies of voltage regulators and compare between them. In the following part, these metrics are defined and explained in some detail along with some factors affecting them.

- **Integrability:**

  This metric measures the ease of integrating voltage regulators on chip and whether the voltage regulator topology under inspection has bulky components that introduce challenges to integrate on chip. Usually, Switch-mode voltage regulators use energy storage elements (or charge transferring elements) which are area consuming. These components can be integrated on chip either by using standard CMOS process or by using some special additional masks with added cost. Another issue is the performance of these components when integrated on chip and to what extent the voltage regulator topology is capable of overcoming the parasitic losses associated with these components. In most cases, the quality factor of on-chip charge transferring components is less than that of their off-chip counterparts. This metric measures how much the VR topology is capable of overcoming these limitations such that its performance is not affected so much when it is integrated on-chip. This metric also measures the level of integration of the voltage regulator circuit; whether it is fully integrated on chip or there are some components in package or off chip.

- **Efficiency:**

  It is considered the most important metric of voltage regulators because it represents the losses that happen inside the voltage regulator. It is defined as total output power from the converter over total input power to the converter:

$$\eta = \frac{P_{out}}{P_{in}} \tag{2.1}$$

  The output power is less than the input power by the amount of power loss that occurs inside the voltage regulator. Basically, the losses inside the voltage regulator are divided into two main types: the conduction losses and the switching losses. The conduction losses P_{cond} is given by:

$$P_{cond} = \sum_i I_{rms,i}^2 R_{par,i} \tag{2.2}$$

  The switching losses come mainly from charging/discharging behavior of gate capacitance of switches when they are turning on and off and the parasitic bottom-plate capacitance of flying capacitors being charged/discharged during the switching behavior of the regulator. In general, any parasitic capacitance at any switching node inside the voltage regulator may cause switching losses.

$$P_{switch} = \sum_i V_{sw,i}^2 C_{par,i} F_{sw,i} \tag{2.3}$$

  where $C_{par,i}$ is the parasitic capacitance being charged/discharged at a frequency of $F_{sw,i}$ and with a voltage swing of $V_{sw,i}$.

- **Output voltage ripples:**

  The output voltage ripples have a direct relation with output capacitor size as well as current ripples going inside the output capacitor. It is more fair to compare between output voltage ripples of different VR topologies using same output capacitor size so that the real capability of the topology to reduce output voltage ripples is measured. The output current from any

voltage regulator circuit can be modeled as a DC value representing the load current drawn by the load circuit plus some ripples imposed on this DC value because of charging/discharging behavior of the voltage regulator. These ripples (i_c) are suppressed by the output capacitor so that the final DC value goes to the load circuit as shown in figure 2.1. These current ripples add or subtract some charges from output capacitor causing the voltage on the output capacitor to change and hence ripples appear on output voltage.

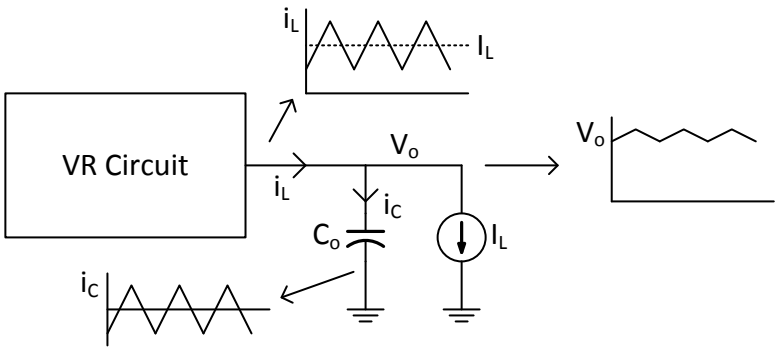


FIGURE 2.1: Output voltage ripples in a voltage regulator

The conclusion is that the current ripples coming out from a VR circuit has a direct relation with output voltage ripples. Recall that the current ripples have a direct impact on efficiency as well. Hence, reducing current ripples in general would help in enhancing both efficiency and output voltage ripples of the voltage regulator. Therefore, the output current ripples of a VR circuit are considered a key factor in determining the performance of a voltage regulator.

- **Power density:**

  It is the maximum amount of output power delivered by a VR over the area consumed by this VR. Since switch-mode voltage regulators depend on energy-storage elements in their operation, they are consuming considerable

amount of silicon area on chip. The higher the power density, the less the area it is consuming on chip for same output power.

The area consumed by a VR on chip has a direct relation with its maximum output power capability. For high output power, large storage elements are required to handle this large power. Large elements mean large associated parasitics causing more losses. The other option is to increase the switching frequency to compensate for small storage elements and allow for higher power densities. However, increasing the switching frequency means higher switching losses. Therefore, there is a strong tradeoff between the power density and the efficiency of a voltage regulator.

- **Regulation Capability:**

  The two main regulation schemes used to control output voltage value are Pulse Width Modulation (PWM) technique where the duty cycle is the main controlling parameter of output voltage and Pulse Frequency Modulation (PFM) technique where the switching frequency is the main controlling parameter of output voltage. The PWM scheme has its well-known developed methodologies and techniques over the time compared to frequency-based scheme [11].

  In some cases, the regulation of output voltage can be done by changing the configuration of the voltage regulator topology. This is considered a coarse tuning of output voltage. A fine tuning method should be added on top of that so that a precise control of output voltage is possible. In some other cases, the regulation is done by changing the size of the charge transferring components of the voltage regulator (i.e. switches, capacitors and/or inductors).

  One of the most important aspects to measure the regulation capability is whether the performance of the regulator is affected when deviating from normal operation points of the voltage regulator. In lossy regulation schemes,

the performance of the regulator degrades quickly when deviating from target operation points. This happens when the losses in the regulator is a strong function in the parameter used to control the output voltage value. Hence, the power loss becomes a function in output voltage value.

Another important aspect is the output range accessibility. This metric measures whether the whole output voltage range is accessible starting from input voltage down to ground. This is important to support the DVFS feature effectively and improve the power management capability of the system.

- **Transient Response:**

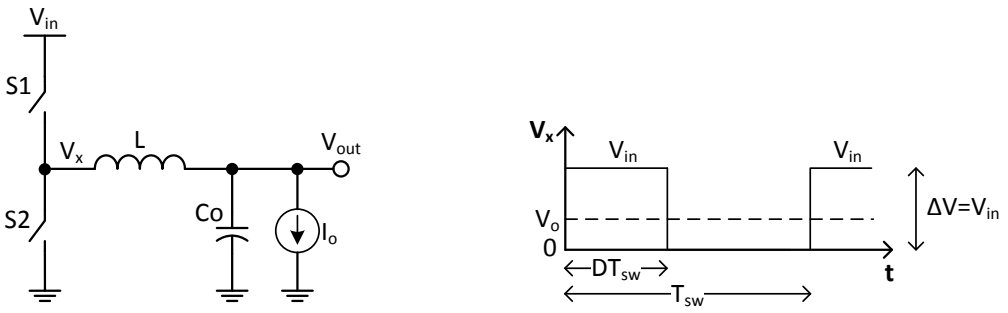
  This metric measures how fast the voltage regulator responds to changes in load current or to any sources of variations in the VR circuit so that a minor effect happens on output voltage (i.e. small overshoots or ripples in output voltage). This is of course highly dependent on the controller design, but the VR topology itself plays an important role in determining the transient response capability of the regulator. For example, inductors do not allow for fast changes in current flowing in them while the capacitors allow. Regulators that have an inductor in the path from input node to output node would have slower transient response especially when large inductor sizes are used. This metric is more important when the VR is supplying circuits that are operating at high frequency and are frequently changing their operation modes (e.g. between active and sleep modes).

There may be other metrics as well but the above mentioned ones are considered the most important to compare between integrated voltage regulators. In the following sections, a review on the two basic types of voltage regulators is provided based on the abovementioned metrics.

2.3 Inductor-based Voltage Regulators

In inductor-based voltage regulators, conventionally known as buck converters, the inductor is used as the main charge transferring component. Their main working principle is based on charging the inductor in one phase then discharging it in the next phase so that the charge is transferred from input node to output node but with a controllable ratio between V and I of output power and with a condition that output voltage is less than input voltage.

Figure 2.2(a) shows the circuit of a conventional buck converter. A switching voltage waveform is generated at the inductor input, as shown in figure 2.2(b), using two switches that switch on and off in a complementary way. After that, the inductor and output capacitor, working as a LPF, take the average of this switching voltage waveform and generate a regulated output voltage. Regulation of output voltage is done by a duty cycle (i.e. PWM scheme) which controls the average value of the switching voltage waveform at the inductor input.



(a) (b)

FIGURE 2.2: Conventional buck converter: (a) circuit structure (b) switching voltage waveform (V_x)

The charging/discharging behavior of the inductor causes ripples in the inductor current. The inductor current ripples are one of the key quantities of buck converters because it is affecting its performance in many aspects. First of all,

these inductor ripples cause the RMS value of inductor current to be higher than its average value. Hence, more losses are dissipated in the parasitic resistances of the regulator according to equation 2.2. Moreover, these inductor current ripples are going inside the output capacitor causing more output voltage ripples.

One way to characterize these inductor current ripples is to calculate its worst case peak-to-peak value. A general relation for any inductor peak-to-peak current ripples is derived here where the input to the inductor is a waveform switching between two voltage levels V_1 and V_2 and the output voltage of the inductor is fixed at certain value (i.e. output voltage of VR) as shown in figure 2.3. In this case, the peak-to-peak current ripples are given by:

$$\Delta i_{L,p-p,g} = \frac{\Delta V D(1-D)}{L F_{sw}} \tag{2.4}$$

where D is the duty cycle of the switching waveform at the inductor input, F_{sw} is the switching frequency of the voltage waveform and ΔV is the voltage difference between maximum voltage level (V_1) and minimum voltage level (V_2) of the switching voltage waveform.

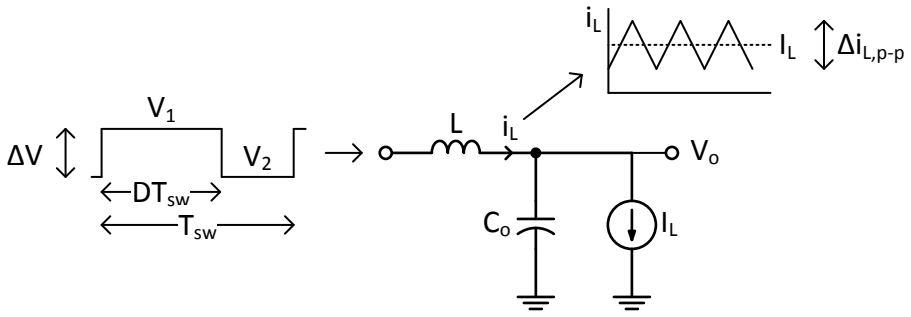


FIGURE 2.3: Inductor current ripples due to a switching voltage waveform at inductor input

Generally, as seen in equation 2.4, the inductor peak-to-peak ripples are a function in duty cycle. The worst case inductor peak-to-peak ripples occurs when duty cycle is equal to half and in this case is given by:

$$\Delta i_{L,p-p} = \frac{\Delta V}{4LF_{sw}} \tag{2.5}$$

For conventional buck converter, ΔV equals $(V_{in} - 0)$ as shown in figure 2.2(b). In this case the worst peak-to-peak current ripples are given by:

$$\Delta i_{L,p-p} = \frac{V_{in}}{4LF_{sw}} \tag{2.6}$$

There are two working modes in the conventional buck converter which are the Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). In CCM, all the inductor waveform is above zero which means no negative current is going back form output capacitor to power supply rails through the inductor. This happens when $(I_L > \frac{1}{2}\Delta i_{L,p-p})$, in this case the buck converter is operating in CCM for the whole duty cycle range. As the average load current (I_L) starts to decrease, at some point, the inductor waveform starts to go under zero. Therefore, at light load currents or large current ripples, the buck converter is most likely operating in DCM. In this case, negative current goes back form output capacitor to power supply rails causing more conduction losses. To prevent these negative current losses, a DCM control loop to switch off the switches before the inductor current goes under zero is required.

2.3.1 Performance Evaluation

The inductor-based voltage regulators have an advantage that they are inherently lossless, which means if all of their components are ideal, its efficiency would be 100%. That is why they are leading off-chip voltage regulators where their

efficiency can reach up to 97% [12]. This high efficiency can be achieved by using large inductors (to reduce conduction losses due to current ripples) and decreasing the switching frequency (to reduce switching losses).

However, this is not the case when it comes to integrating buck converters on chip. On-chip inductors have limitations on their sizes as well as having poor quality factors compared to their off-chip counterparts. That is why they tend to use small inductors on chip and increase the switching frequency to accommodate for inductor size reduction as depicted in equation 2.5. However, there are limitations on the maximum operating switching frequency of voltage regulators on chip. One of these limitations is the designing of main and secondary control loops of buck converters at such high frequencies [13]. For example, designing of some control circuits like DCM control loop to prevent negative currents is a challenging task [14] where precise control of on/off time of switches is required. Another example is the dead time implementation circuit that has to be carefully designed to prevent short circuit current in the VR. Besides all of that, a high switching frequency means substantial switching losses in the VR.

To gain more insight on inductor current ripples problem, an example with practical values on the design of integrated buck converters is provided. Usually, the on-chip spiral inductor size used in integrated voltage regulators is in the range of 1nH and cannot exceed 10nH [15]. Above that size, the equivalent series resistance (ESR) of the inductor would cause substantial conduction losses that affect the VR performance so much. Suppose that the regulator is operating at a switching frequency of 500MHz which is the maximum reported until now for a digital controller for buck converters [16]. The regulator has an input voltage of 1.2V and is to supply a load current of 100mA. For a 1nH inductor, the worst case peak-to-peak current ripples is 0.6A according to equation 2.5 which is six times the average load current. This means very high RMS value of inductor current causing high conduction losses. The best performance of buck converter is usually obtained at the region around boundary of CCM and DCM modes (i.e.

$I_L \approx \frac{1}{2}\Delta i_{L,p-p}$) [14] which means this design is far enough from optimum point when using this inductor size and switching frequency.

That is why on-chip inductor-based voltage regulators are used mainly for high power applications where the load current would have comparable ration with inductor ripples hence the power loss due to ripples does not dominate the whole losses. In low power applications, the unavoidable current ripples will cause considerable amount of losses. Therefore, inductor-based voltage regulators are used mainly for applications with output power higher than 100mW [17].

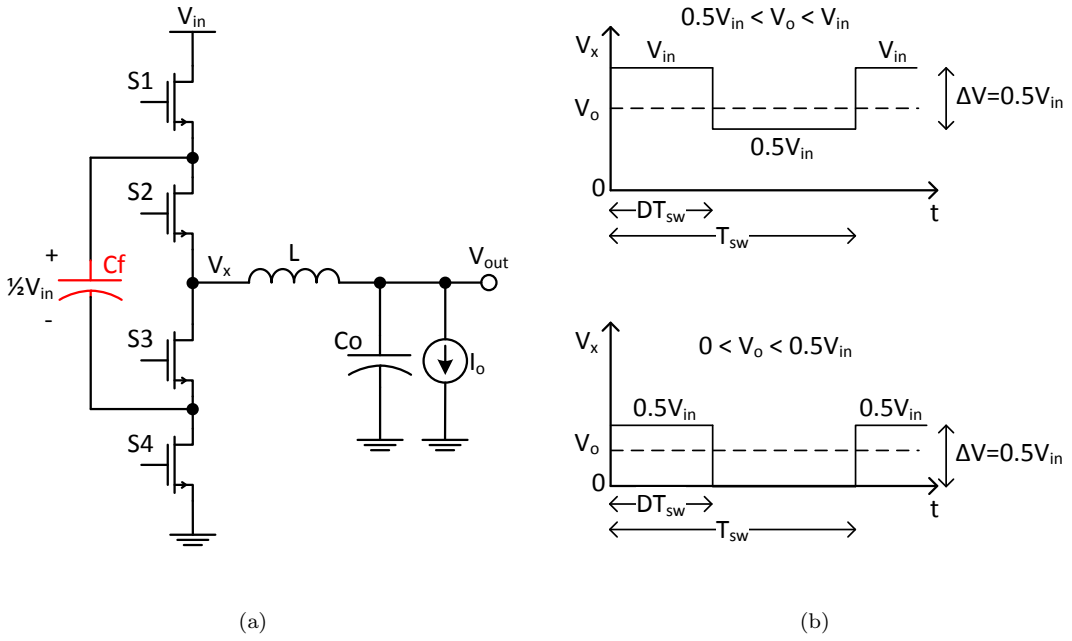
Figuring out a way to reduce inductor ripples without increasing inductor size would be of great benefit to integrated buck converters. In general, reducing inductor ripples can be done by:

1. Increasing inductor size (Reached its limit for on-chip inductors)
2. Increasing switching frequency of the regulator (limitations on-chip)
3. Reducing maximum voltage drop at the inductor input.

The third point (reducing ΔV at inductor input) seems promising to help overcome the limitations associated with integrated buck converters where the first two points have reached their limits for on-chip voltage regulators.

2.3.2 3-level Buck Converter

The 3-level buck converter has been proposed [18–21] as a trial to overcome the main limitation of inductor-based voltage regulators (i.e. inductor size) and taking a step forward towards integrating them on-chip. Its circuit structure is shown in figure 2.4(a). A new voltage level of $0.5V_{in}$ is introduced at the input of the inductor by using a flying capacitor balanced at $0.5V_{in}$. It has two operation zones according to the required output voltage value as shown in figure 2.4(b). In



(a) (b)

FIGURE 2.4: 3-level buck converter: (a) circuit structure (b) switching voltage waveform (V_x) in each of two output ranges

the first zone, the node at the inductor input (V_x) is switching between V_{in} and $0.5V_{in}$ where the required output voltage lies between these two voltage levels. In the second zone, V_x is switching between $0.5V_{in}$ and zero. The output voltage value inside each zone is controlled by a duty cycle as seen in figure 2.4(b).

The 3-level buck converter features smaller voltage drop at the inductor input and an increased effective switching frequency allowing for smaller inductor sizes for the same peak-to-peak current ripples. Actually, the voltage drop on the inductor is reduced by two and the effective switching frequency is increased by two which theoretically allows for reducing the inductor size by 4 for the same inductor ripples according to equation 2.5.

The 3-level buck converter can help in realizing on-chip voltage regulators using on-chip inductors with efficiency higher than that of conventional buck converter. Some circuit implementation for 3-level buck converter on CMOS standard technology has been done [22, 23] achieving a peak efficiency of 77% [22]. However,

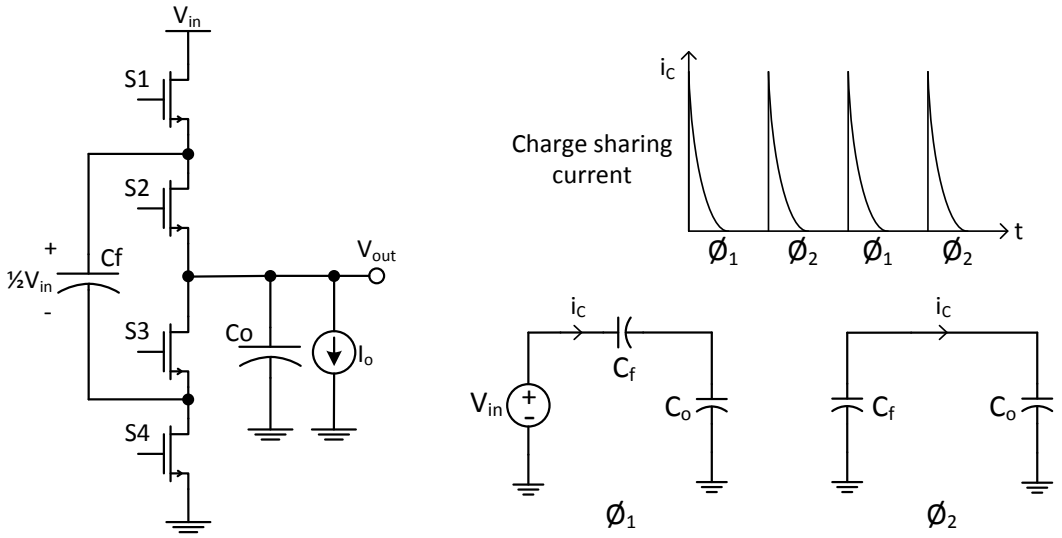
this amount of inductor size reduction achieved in 3-level buck converter is beyond that required for efficient integration and the inductor size is still limiting the performance of on-chip inductor-based voltage regulators. Further decrease of inductor size without affecting the operation of the voltage regulator would help in boosting the performance of integrated buck converters.

2.4 Capacitor-based Voltage Regulators

In capacitor-based voltage regulators, sometimes known as charge pumps or switched capacitor voltage regulators (SCVRs), flying capacitors are used as the main charge transferring components between input and output nodes where in one phase these flying capacitors are charging/discharging then in next phase they are discharging/charging. Their main principle is based on providing the required voltage difference between input and output nodes using flying capacitors.

Capacitors, unlike inductors, cannot support arbitrary voltage difference on them when going between phases (i.e. the voltage on the flying capacitor cannot change instantaneously). Consequently, switched capacitor voltage regulators have normal fixed values for output voltage where the ratio between this output voltage and input voltage is called the conversion ratio this topology is providing. This is achieved by connecting the flying capacitors in a certain way that provide the required voltage difference between input (or ground) and output nodes in the two phases. Therefore, the normal output voltage of a SCVR is determined by the topology structure itself where flying capacitors are forced to balance at certain values. For a SCVR topology to be able to provide more conversion ratios, more capacitors and switches have to be added to allow for more configurations of the topology [24].

Figure 2.5(a) shows the simple 2:1 SCVR topology. The normal output voltage of this topology is $0.5V_{in}$ where the flying capacitor is forced to balance at $0.5V_{in}$.



(a) (b)

FIGURE 2.5: Switched capacitor voltage regulator: (a) circuit structure (b) two phases of the circuit and the charge sharing current waveform

Figure 2.5(b) shows the two phases of the circuit and the charge sharing current between flying capacitor and output capacitor that occurs at the start of each phase.

Besides the coarse tuning of output voltage done by conversion ratio selection, fine tuning of output voltage inside each conversion ratio can be done using several techniques. The main technique is by using the switching frequency (i.e. PFM) [25–27] where as the switching frequency scales down, the output voltage goes lower than its normal value. Other regulation techniques exist like regulation using switch resistance modulation [28]. However, these techniques sometimes have non-linear characteristics that may affect the response of the regulator and cause instability in the control loop [29].

2.4.1 Performance Evaluation

Capacitor-based voltage regulators are gaining more attention nowadays as they are easy integrable on chip than inductor-based ones using standard CMOS technology. This is because the advances made in integrating capacitors on-chip with high density and high quality factor exceed that of inductors. However, capacitor-based voltage regulators have some fundamental limiting factors.

One main limitation factor in switched capacitor voltage regulators is that they are inherently lossy which means if all components of the regulator are ideal, the regulator efficiency does not reach 100%. This is mainly because some energy has to be lost in the charge sharing process that occurs between flying capacitors and output capacitor at each phase.

At the start of each phase, there is a mismatch (ΔV) between input voltage, flying capacitor voltage and output capacitor voltage. This happens because capacitors at the end of the previous phase are balanced at values that do not satisfy the Kirchhoff's Voltage Law (KVL) loop at the start of the next phase. Since capacitors cannot support arbitrary or flexible voltage on them like inductors, this mismatch (ΔV) is then supported by the parasitic resistances of the circuit causing large current to flow in these resistances. This current is the charge sharing current that transfers the charges between capacitors until they are balanced at values that satisfy the KVL loop of that phase. This process is repeated at the start of each phase where the charge transferring current starts with a very large peak at the beginning of each phase, then starts to decay as the voltages on flying capacitors are approaching their normal balanced values in that phase as shown in figure 2.5(b). The charge sharing current has a large RMS value that causes large conduction losses.

Generally, the conduction losses inside switched capacitor voltage regulators

have two main limits depending on the switching frequency relation with time constants of the switched capacitor circuit (switches and flying capacitors) [24, 30, 31]. If the switching frequency is low enough, then there is enough time for complete charge sharing to take place in each phase. In this case, the charge sharing losses are dominating the total conduction losses of the regulator. Therefore, they are called the Slow Switching Limit (SSL) losses where the output resistance of the voltage regulator (representing conduction losses) in this case is given by:

$$R_{SSL} = \frac{m}{C_f F_{sw}} \tag{2.7}$$

where m is a constant determined by the switched capacitor topology. Therefore, these losses are a strong function in switching frequency itself (F_{sw}) and the flying capacitor size (C_f). These losses are what makes switched capacitor voltage regulators inherently lossy.

If the switching frequency is high enough, then there is no time for complete charge sharing to take place between capacitors in each phase. In this case, the losses due to switch parasitic resistance (R_{on}) are dominating the total conduction losses of the regulator. These losses are called the Fast Switching Limit (FSL) losses and in this case the output resistance of regulator is given by:

$$R_{FSL} = nR_{on} \tag{2.8}$$

where n is a constant determined by the switched capacitor topology. At moderate frequencies, both types of losses exist and the total conduction losses are a combination of both of them. In this case, the output resistance that represents the total losses dissipated in the regulator is given by:

$$R_{out} = \sqrt{R_{SSL}^2 + R_{FSL}^2} \tag{2.9}$$

The main regulation scheme of capacitor-based voltage regulators is by adjusting the switching frequency where as the frequency scales down, the output voltage goes lower. This regulation scheme is lossy and affects the regulator performance in terms of efficiency and output voltage ripples. Fast degradation of efficiency and output voltage ripples occurs once deviating from target operation point as the frequency is scaling down. This is because conduction loss is a strong function in switching frequency specially when operating in SSL region as discussed previously in equation 2.7. In this region, as the frequency scales down, the voltage mismatch between capacitors at the start of each phase becomes larger causing higher charge sharing current between capacitors. This current has higher RMS value causing more conduction losses and hence lower efficiency. Additionally, this current is filtered out by the output capacitor causing higher output voltage ripples. Besides that, this regulation scheme still does not have its well-known developed techniques like PWM regulation scheme.

Another limitation in capacitor-based voltage regulators is that the whole input range is not accessible starting from zero to V_{in} or is accessible with lower efficiency if it is far from normal operation points. To access the whole range with higher efficiency, multiple conversion ratios that cover this operation region must be added [24, 32]. Increasing the number of conversion ratios, a certain topology is providing, means adding more capacitors and switches associated with their parasitics and hence the performance is degraded in general. A balance between the number of conversion ratios and the performance of the topology should be made.

On the other hand, switched capacitor voltage regulators have two main advantages. The first advantage is that they are easy integrable on chip because there are no large magnetic components as the case in inductor-based voltage regulators. The second advantage is that they have faster response than inductor-based voltage regulators.

2.4.2 Switched Capacitor Regulator with an Inductor

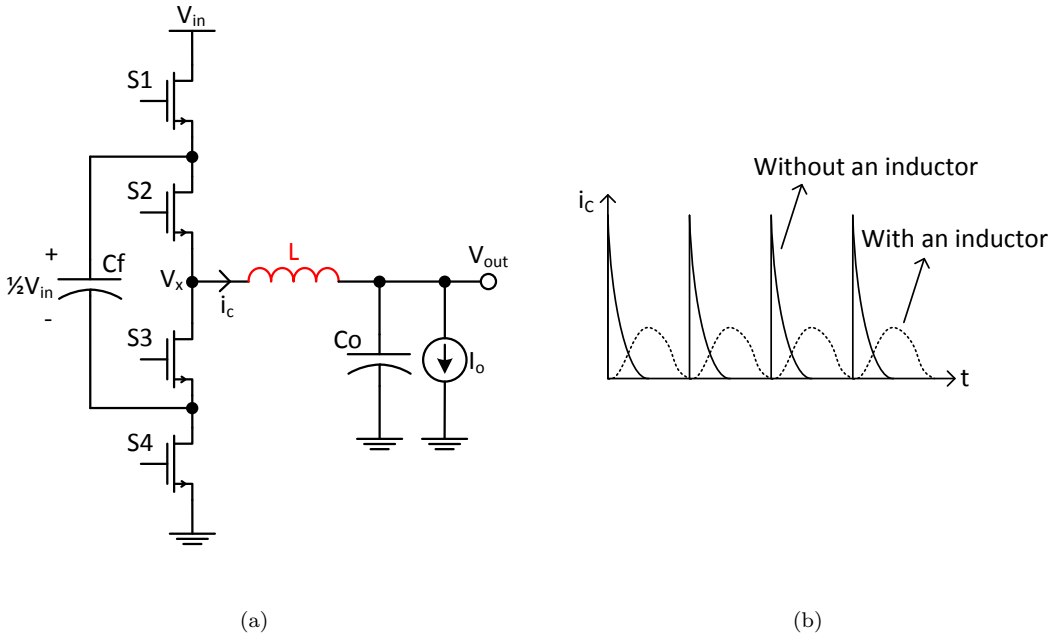


FIGURE 2.6: Switched capacitor voltage regulator with an inductor: (a) circuit structure (b) charge sharing current between C_f and C_o

An attempt to overcome the problem of charge sharing losses in capacitor-based voltage regulator is by adding a small inductor between the flying capacitor and the output capacitor [33] to save some charge sharing losses between these two capacitors as shown in figure 2.6(a). This small inductor helps in boosting the voltage regulator efficiency.

The inductor handles the (ΔV) difference between the flying capacitor voltage and the output capacitor voltage at the start of each phase. This is because of the ability of the inductor to support arbitrary voltage drop on it. This voltage drop on the inductor is translated into current ripples that are much smoother than that of SCVR without inductor. Figure 2.6(b) shows a comparison between charge sharing current with and without the inductor. Thus, the inductor works mainly as a charge transferring controller between the flying capacitor and the output capacitor. The charges are transferred gradually rather than almost once at the

start of the phase. Therefore, the charge sharing current has lower RMS value. This helps in saving some of charge sharing losses that happens in conventional switched capacitor circuits.

This technique worked somewhat on solving the problem or the limitation of charge sharing losses in switched-capacitor voltage regulators. However, other limitations of switched capacitor voltage regulators still exist like fast degradation in performance when deviating from target operation point (i.e. lossy regulation scheme).

2.5 Hybrid Structures

A conclusion can be extracted from the previous discussion. To help overcoming the main limiting factor of inductor-based voltage regulators which is the inductor size, a secondary flying capacitor is added to the main topology of conventional buck converters to generate an additional voltage level that helps in reducing inductor size as shown in figure 2.4(a). This means that inductor-based voltage regulators are adding capacitors to overcome their limitations. On the other hand, to help overcoming the main limiting factor of switched capacitor voltage regulators which is the SSL losses, a small inductor is added between flying capacitor and output capacitor to restore some of these losses as shown in figure 2.6(a). This also means that capacitor-based voltage regulators are utilizing inductors to help overcoming their limitations.

By comparing the two circuits in figures 2.4(a) and 2.6(a), we can notice that both of them have a typical circuit structure. The difference is in the operation principle and the controlling technique used to run each circuit. It seems that each type of voltage regulator is evolving towards the other type which means that the optimum point is a structure that is a combination between both types of voltage regulators.

Table 2.1 summarizes the features and issues of each type of voltage regulators. It can be noted that each type is providing complementary solutions to issues facing the other type. Therefore, a hybrid structure between inductor-based voltage regulators and capacitor-based voltage regulators, that is completely merged, may offer an optimum solution for challenges facing integrated voltage regulators.

TABLE 2.1: Summary of features and limitations of both types of voltage regulators

	Inductor-based Voltage Regulators	Capacitor-based Voltage Regulators
Features	• Inherently lossless • Efficient regulation scheme • High efficiency over wide range of output voltages	• Easy integrable • Fast dynamic response
Limitations	• Inductor size causing problems in integration • Slower dynamic response due to existence of inductor	• Inherent losses • Fast degradation of performance when deviating from normal operation points (Lossy regulation scheme) • Limited access to output range

Chapter 3

Multilevel Multistate Voltage Regulator

3.1 Introduction

It is concluded in the previous chapter that a hybrid voltage regulator structure should offer the optimum solution for challenges facing modern voltage regulators. In this chapter, a proposed multilevel multistate voltage regulator (MMVR) is introduced which has a hybrid structure between inductor-based and capacitor-based voltage regulator. The general structure and the working principle of the proposed voltage regulator are explained. After that, some operation conditions, essential for proper operation of the regulator, are defined. Techniques to operate the voltage regulator and regulate the output voltage are illustrated in detail with the different controlling parameters used to achieve that. Some aspects related to the multilevel multistate voltage regulator like the flying capacitor stability issue are discussed.

After introducing the proposed voltage regulator with some definitions, detailed analysis on the proposed voltage regulator along with comparisons with the two

main types of voltage regulators are provided. This analysis proves that the proposed voltage regulator offers potential solutions to most of problems facing both types of voltage regulators.

3.2 General Structure and Working Principle

3.2.1 General Structure

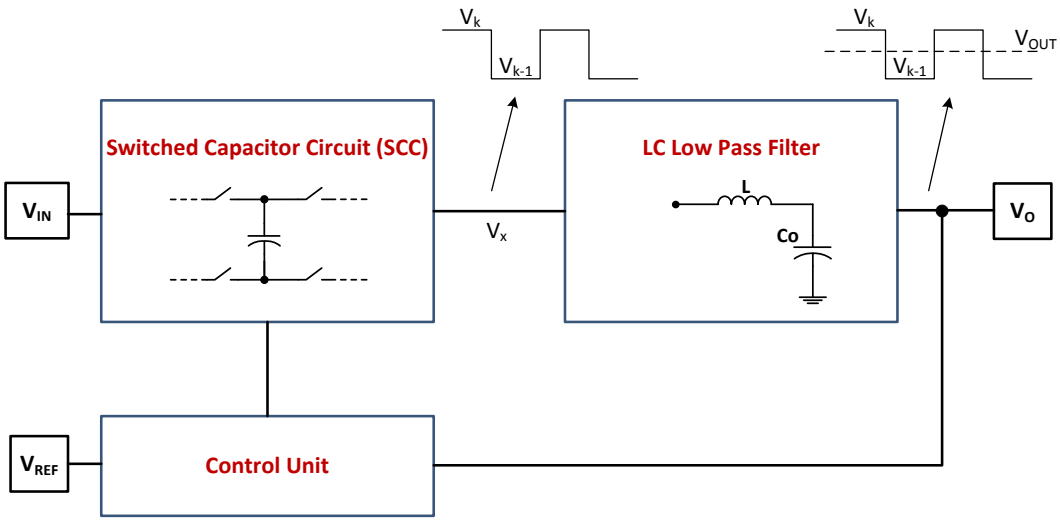


FIGURE 3.1: General Structure of the proposed Multilevel Multistate Voltage Regulator (MMVR)

Figure 3.1, shows a block diagram for the general structure of the proposed voltage regulator. It consists mainly of three blocks: a switched capacitor circuit (SCC), a low pass filter (LPF) and a controller. The first block is a multi-ratio switched capacitor circuit (SCC) that is capable of delivering a number of different output voltage levels from an input voltage. The switched capacitor circuit is periodically switching its output between two different adjacent voltage levels generating a switching voltage waveform at its output. The second block is a low pass filter that takes the average of the voltage waveform generated at its input

and provides a regulated output voltage. It consists mainly of an inductor followed by an output capacitor (decoupling capacitor). The third block is a controller that is responsible for generating the different configurations for the SCC along the operation timeline of the VR. The controller takes the output voltage and the target reference voltage as an input and generates the switch driving waveforms as an output. More details about the circuit operation are described in the following discussion.

The SCC consists of a combination of switches and flying capacitors and is capable of providing n different voltage levels at its output by changing its configuration. Each voltage level is provided by a certain conversion ratio where each conversion ration consists of some phases (i.e. configurations for the SCC) to provide this voltage level. Therefore, in other words, the SCC is capable of providing different conversion ratios. The voltage levels that the SCC is providing include the two power supply rails V_{in} and Gnd. They are provided by a direct connection between input and output nodes of the SCC without involving any flying capacitors in the process.

It is worth mentioning that the SCC is just a switched capacitor circuit (SCC) not a complete switched capacitor voltage regulator (SCVR) as it does not have an output capacitor and it does not have any regulation capability when used alone. It is just a combination of switches and capacitors that is providing non-regulated voltage levels.

The Low pass filter consists of an inductor and the normal decoupling output capacitor of the voltage regulator. The inductor here is of a reduced size as will be illustrated later. The decoupling output capacitor works on reducing the output voltage ripples as the case in any normal voltage regulator. This low pass filter block does not have any regulation capability (i.e. no switches), it just take the average of the switching voltage waveform generated at its input.

This general structure of the proposed voltage regulator can be used to build step-up, step-down or step T up/down converters. It is all dependent on the nature of the voltage levels the SCC is capable of providing. For a step-up converter,all the voltage levels the SCC is providing are higher than or equal to input voltage. In a step-down converter, the SCC is providing voltage levels lower than the input voltage where the highest voltage level is considered to be the input voltage and the lowest voltage level is considered to be the ground. In a step-up/down converter, some voltage levels are higher than the input voltage and some are lowers.

Therefore, we can assume that the lowest voltage level available from the SCC in a step-up converter is the input voltage. In a step-down converter, the highest voltage is the input voltage and the lowest voltage level is the ground. In a step-up/down converter, the input voltage level lies in between the highest voltage level and the lowest voltage level the SCC is providing. In this work, we will focus on the step-down structure where all the voltage levels the SCC is providing are less than V_{in}. However, the same concepts and analysis mentioned here can be applied directly on the other two types.

3.2.2 Operation Principle and Output Regulation

In this part, we will explain how the generation and regulation of output voltage is done specifically. The switched capacitor is configured to switch its output periodically between two adjacent output voltage levels where the desired output voltage lies between these two voltage levels. According to this, we can find that the regulator has different operation regions. In each operation region, the switched capacitor circuit is changing its output between two certain voltage levels. Based on the desired output voltage value, the appropriate operation region can be selected where the output voltage lies between the two voltage levels this operation region is providing. This is considered a course tuning for output voltage level.

Suppose that we have a switched capacitor circuit capable of generating n conversion ratios which means n different output voltage levels including the two supply rails (i.e. conversion ratio of one or zero). This means a total number of (n-1) operation regions where in each operation region the SCC is switching between two adjacent voltage levels. Figure 3.2 shows the different operation regions of the regulator in this case. The operation region one (OP_1) is when the SCC changes its voltage between V_1 and V_2. The second operation region (OP_2) is when the SCC changes its voltage between V_2 and V_3 and so on. The last operation region OP_{n-1} is when the SCC is switching its output between V_{n-1} and V_n. Usually, V_1 is the 'V_{in}' voltage level and V_n is the 'Gnd' voltage level.

Fine tuning for output voltage level inside each operation region is done by a duty cycle which determines the relative duration between the first voltage level and the second voltage level. This duty cycle controls the average value of the switching waveform generated from the SCC and is called the main duty cycle (D). The low pass filter then takes the average of this switching voltage waveform generating the target regulated output voltage value. TO sum up, the regulation of the output voltage is done on two steps. The first step is the operation region selection. The second step is controlling the output voltage level inside that operation region by the main duty cycle value.

Each voltage level or conversion ratio from SCC is provided by certain number of phases which is usually two. However, there are some SCC topologies where each voltage level is provided by more than two phases but the analysis. The analysis in this work is limited to the case of voltage levels provided by two phases only. A phase means a certain configuration for the switches inside the SCC that result in a certain connection between capacitors, input node, ground node and output node.

The operation timeline of the regulator consists of several switching cycles repeated as long as the circuit stays in that operation region. A one switching cycle

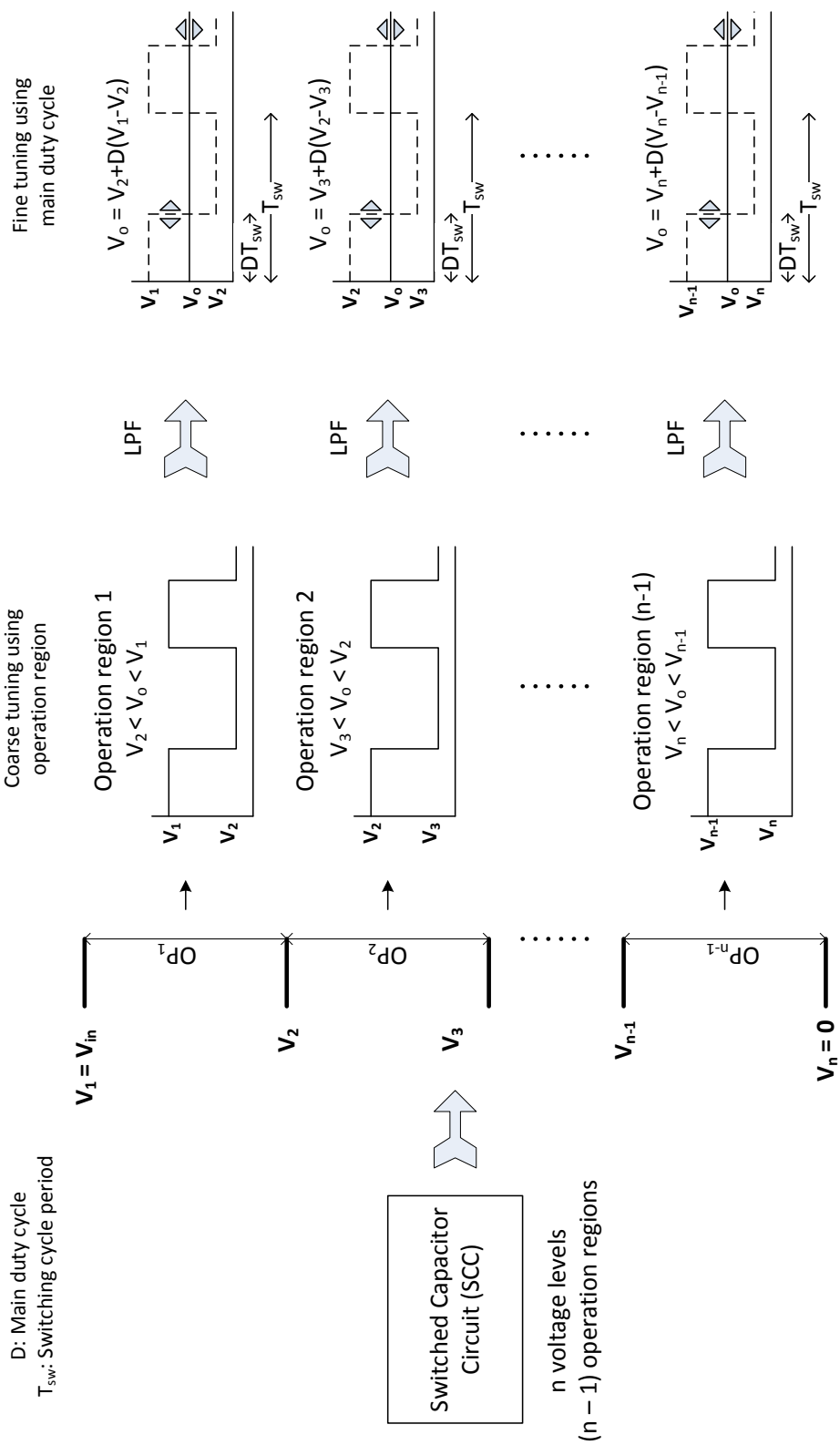


FIGURE 3.2: Different operation regions for the proposed multilevel multistate hybrid voltage regulator

has a duration period (T_{sw}) equal to one over the main switching frequency of the regulator (F_{sw}) and is divided into a number of states where each state is assigned to a certain phase from the SCC. Each state has its relative duration to the main switching cycle duration. The first group of states in the switching cycle is assigned to phases of the first voltage level while the remaining states are assigned to phases of the second voltage level where the first and second voltage levels are the two voltage levels of the operation region the regulator is operating at.

Figure 3.3 shows the switching cycle of the regulator inside a certain operation region in case that each voltage level is provided by two phases. In this case, a one switching cycle is divided into four states where the first two states are assigned to phases of first voltage level while the second two states are assigned to phases of second voltage level.

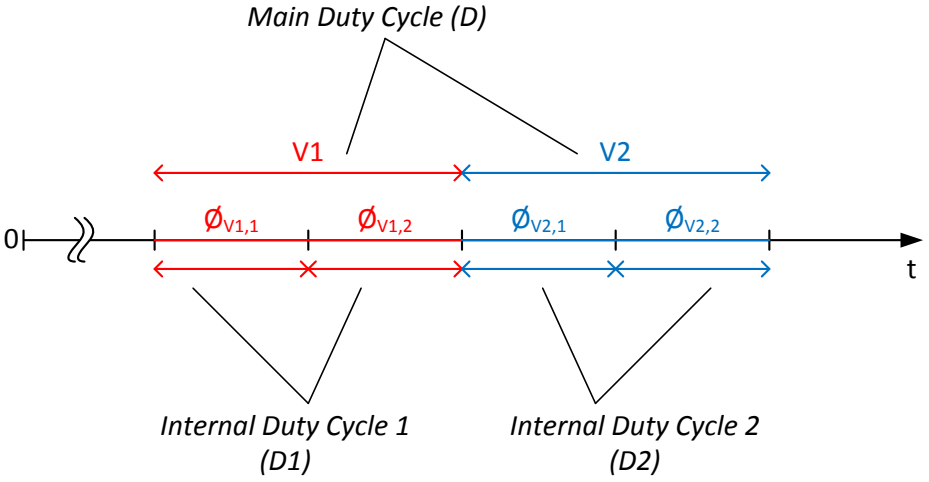


FIGURE 3.3: Switching cycle of MMVR inside a certain operation region

Each voltage level has an inner duty cycle that represents the relative duration between the two phases of that voltage level. Therefore, each operation region has two internal duty cycles (D_1 and D_2) representing the relative duration between phases of two voltage level of that operation region besides the main duty cycle (D) representing the relative duration between the two voltage levels of that operation

region as shown in figure 3.3. The internal duty cycle values are important for ensuring stability of flying capacitors inside the SCC as will be discussed in the following section.

The internal duty cycles as well as the main duty cycle completely define the duration of each state inside switching cycle with respect to the duration of one complete switching cycle (T_{sw}).

3.2.3 Controlling Parameters

The control parameters of the MMVR are divided into two categories: main control parameters and secondary control parameters. The main control parameters are responsible for regulating the output voltage and keeping it at the desired value. While the secondary control parameters are responsible for ensuring a proper operation of the converter and maximizing its performance during different operation and loading conditions.

The main control parameters are the operation region responsible for coarse tuning of the output voltage level and the main duty cycle responsible for fine tuning of the output voltage inside a certain operation region. Therefore, the main regulation technique in the proposed voltage regulator is a PWM technique.

The secondary control parameters include internal duty cycles and main switching frequency. They are responsible for flying capacitors stability inside the SCC. For correct operation of the circuit, the flying capacitors are required to balance at their normal values depending on the SCC topology used. For each operation region, there are optimum values for these inner duty cycles, optimum values that keep the average voltage on the flying capacitors balanced at their normal value. For a SCC where each voltage level has a maximum of two phases, then for each operation region there are two inner duty cycles. The first and second inner duty cycle represents the relative duration between the phases of voltage level one and

voltage level two respectively. The switching frequency is not the primary control variable for output voltage regulation. However, it can be used to boost the performance of the converter under different loading conditions. For example, it can scale down with the load current drawn from the regulator so that the performance of the regulator is enhanced at light loads. Table 3.1 summarizes the different controlling parameters and their functions in the MMVR.

TABLE 3.1: Controlling parameters of multilevel multistate voltage regulator

Control Parameter		Function
Primary	Operation region	Coarse tuning of output voltage
	Main duty cycle (D)	Fine tuning of output voltage
Secondary	Internal duty cycles (D_1 and D_2)	Flying capacitor stability and converter performance
	Switching frequency	Converter performance over different operation and loading conditions

3.2.4 Operating Conditions

There are some conditions that should be satisfied for proper and efficient operation of the MMVR. These conditions are listed below:

1. Each conversion ratio in the SCC is provided with a number of phases that enforces the flying capacitor stability at a certain value when operating alone. This means that the flying capacitor has zero degree of freedom when solving KVLs of phases of a certain conversion ratio). All these phases must be used to produce the required voltage level and must be existent in the switching cycle.(in other words) each voltage level has number of phases that must be included to provide this voltage level. All the essential phases for each of the

two voltage levels must be included in one switching cycle to ensure that the two voltage levels are provided

2. The flying capacitors are balanced at the same value in each conversion ratio or voltage level. For example, if the SCC is capable of providing four voltage levels, each flying capacitor must balance at the same value in each voltage level of those four voltage levels. Any voltage level where the flying capacitors are balanced at values different than those of other voltage levels should be excluded and not used inside any operation region. The selected SCC topology should satisfy this condition.

3. The internal duty cycles in each operation region should be adjusted so that flying caps stability is ensured. This is discussed in the next section.

These conditions are to ensure that the circuit is operating correctly under the proposed techniques and methods mentioned in this work. However, some deviations from these rules may be acceptable but will need its own separate analysis to ensure its feasibility and proficiency.

3.3 Flying Capacitor Stability

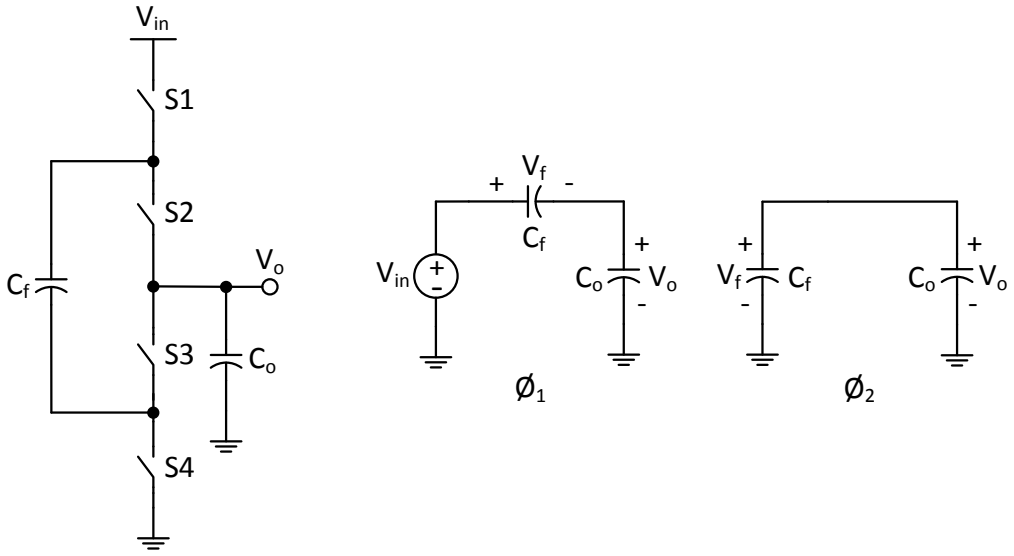
In the proposed multilevel multistate voltage regulator, the flying capacitors' stability is an important aspect for ensuring correct operation and optimum performance of the regulator. The flying capacitor is stable when the average voltage on it is balanced at its normal value which is determined by the SCC topology. Any deviations from these normal values mean that the flying capacitor is instable or is imbalanced and the performance of the regulator is affected. Since an inductor is added in the path from the flying capacitor to the output capacitor, the average voltage on the flying capacitor becomes sensitive to the internal duty

cycle of a conversion ratio (i.e. relative duration between phases of a single conversion ratio). To study the effect of the inductor on the flying capacitor stability, the 2:1 conversion ratio topology with and without an inductor between C_f and C_o is taken as a case study.

The first case to start with is the 2:1 topology without an inductor shown in figure 3.4(a) and its corresponding two phases shown in figure in 3.4(b). At the start of each phase, charge sharing between C_f and C_o occurs causing the flying capacitor to finally balance at a value that satisfies the Kirchhoff's Voltage Law (KVL) in each of the two phases [24]:

$$\text{In } \phi_1: \quad V_{in} - V_f - V_o = 0 \tag{3.1}$$

$$\text{In } \phi_2: \quad V_f - V_o = 0 \tag{3.2}$$



(a) (b)

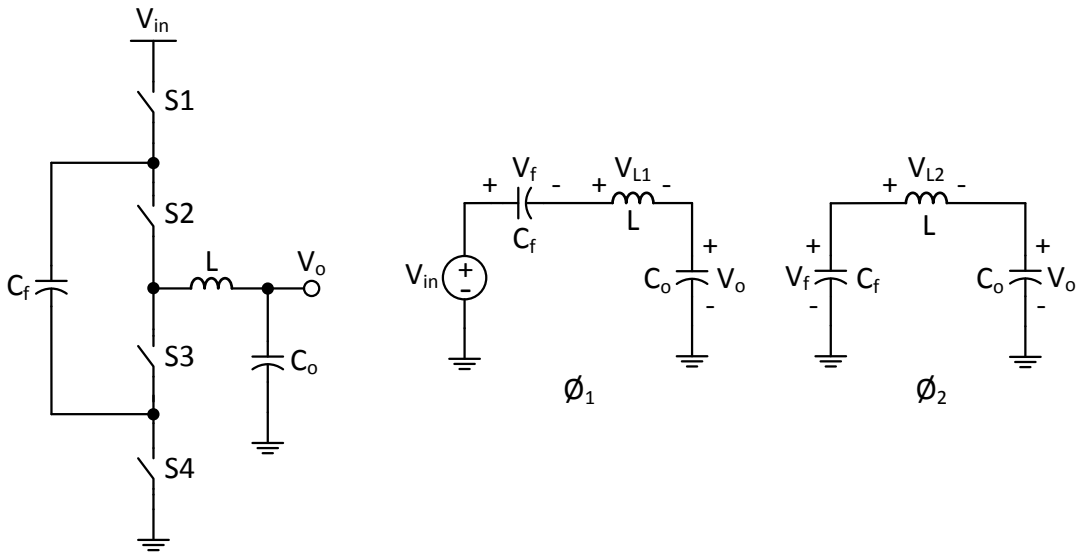
FIGURE 3.4: 2:1 SC topology without an inductor: (a) circuit structure (b) two phases of the circuit

Since the voltage on the flying capacitor cannot change its value instantaneously when going between the two phases, the average voltage on the flying capacitor V_f in first phase should be the same in next phase. Solving the two equations 3.1 and 3.2 in terms of V_f yields:

$$V_f = V_o = 0.5V_{in} \tag{3.3}$$

Therefore, for a first order approximation, the flying capacitor is always balanced at $0.5V_{in}$ regardless the internal duty cycle value (i.e. duration of first phase with respect to second phase). This can be noticed as well from figure 3.6 where when the inductor value approaches zero, the average voltage on the flying capacitor is almost fixed at $0.5V_{in}$ for all the rang of internal duty cycle values. During normal operation, if imbalance occurs at the start of any phase, large current caused by charge sharing between capacitors would cause the flying capacitor to eventually balance at a value that satisfies the two KVLs.

When adding an inductor between C_f and C_o as shown in figure 3.5(a), which is the case in all MMVR circuits, the inductor stores some of the energy to be transferred between C_f and C_o during charge sharing process. The amount of energy stored in the inductor is dependent on the internal duty cycle value. The inductor has a feature that it allows the voltage on it to change instantaneously while the current cannot. This means that the inductor can limit the charge sharing current between C_f and C_o while in the same time allowing the flying capacitor to balance at values different than its normal value without the inductor. In this case, the inductor support the mismatch in voltage caused in each of the two phases. The two KVLs of the two phases of the circuit, shown in figure 3.5(b), are given by:



(a) (b)

FIGURE 3.5: 2:1 SC topology with an inductor: (a) circuit structure (b) two phases of the circuit

$$\text{In } \phi_1: \qquad V_{in} - V_f - V_{L1} - V_o = 0 \tag{3.4}$$

$$\text{In } \phi_2: \qquad V_f - V_{L2} - V_o = 0 \tag{3.5}$$

We can notice that there are some degrees of freedom in the two equations because of V_{L1} and V_{L2}. Since the inductor can support arbitrary voltage on it or in other words the voltage on the inductor can change instantaneously, V_{L1} in first phase is not necessarily equal to V_{L2} in second phase. There values are function in internal duty cycle as well as other circuit parameters (e.g. inductor size). Consequently, according to equations 3.4 and 3.5, the value of V_f becomes a function in internal duty cycle and other circuit parameters. As the inductor size increases, the dependency of the flying capacitor voltage on the duty cycle increases. Thus, the flying capacitor voltage(V_f) is not forced at certain value and can deviate from its normal value calculated when there is no inductor. However,

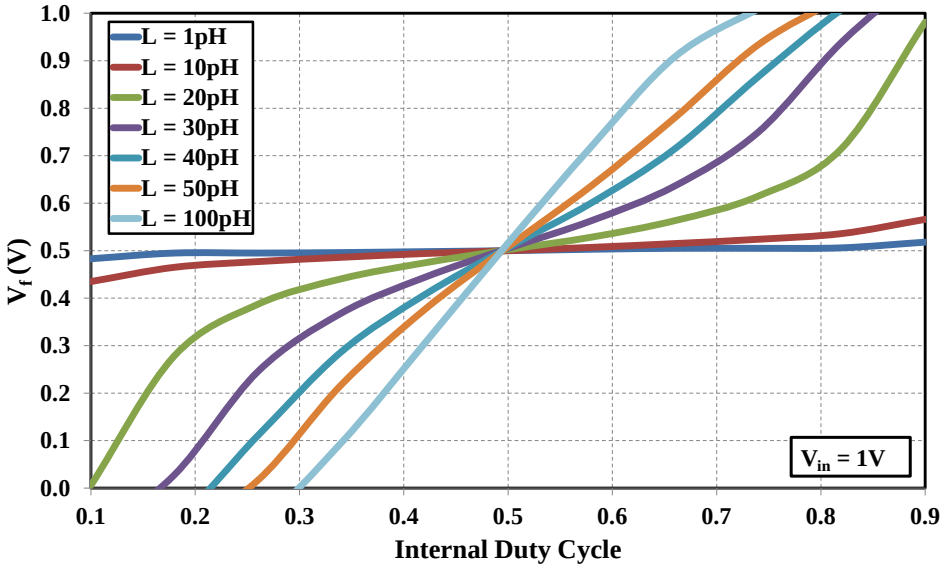


FIGURE 3.6: Average voltage on flying capacitor (V_f) versus internal duty cycle for different inductance values

once the internal duty cycle is equal to the optimum value which is 0.5 in our case, the flying cap would balance at its normal value $0.5V_{in}$, as shown in figure 3.6, irrespective of values of circuit parameters like the inductor size.

The inductor value determines the sensitivity of V_f to internal duty cycle value and other circuit parameters. Figure 3.6 represents the average voltage on the flying capacitor (V_f) versus internal duty cycle (D) for different inductance values. These results are obtained from a SPICE simulation of 2:1 topology. The flying capacitor voltage is almost independent on the duty cycle when the inductor size approaches zero and this is the case in normal switched capacitor voltage regulators. As the inductor size increases, the sensitivity of V_f to D starts to increase as shown in figure 3.6. This is because the larger the inductor size, the larger the arbitrary voltage it can support. Hence, the flying capacitor has more freedom to balance at other values rather than the normal value determined by charge sharing process. This is mainly because the duty cycle controls the charging/discharging time of the flying capacitor. So, if the charging time is larger than the discharging time, the flying capacitor would balance at a value higher than its normal

value and the inductor will support this difference in voltage between the flying capacitor and the output capacitor.

If a mismatch in the flying capacitor voltage occurs, the circuit is still functional but not with the maximum efficiency. This is because this mismatch in V_f causes variations in the output voltage level from SCC. For example, in the 2:1 topology, if the voltage on the flying capacitor (V_f) has a mismatch of ΔV_f from $0.5V_{in}$, the output voltage level from the SCC at the inductor input is not $0.5V_{in}$ during the two phases. It would rather have different value at each phase. In phase one, it would be:

$$V_{x1} = V_{in} - 0.5V_{in} - \Delta V_f = 0.5V_{in} - \Delta V_f \tag{3.6}$$

while in phase two, it is:

$$V_{x2} = 0.5V_{in} + \Delta V_f \tag{3.7}$$

These differences in output voltage levels from SCC, going as an input to the inductor, would cause higher voltage drop on the inductor which in turn result in higher inductor current ripples. Higher inductor current ripples means higher RMS value of inductor current and hence higher conduction losses. Therefore, ensuring that the flying capacitors are balanced at their normal value is good for ensuring that the regulator is giving the optimum performance.

The effect of mismatch in internal duty cycle on circuit performance is maximized for large inductor sizes where small deviations from optimum duty cycle values would cause large changes in V_f value. On the other hand, when the inductor size is small, V_f becomes less sensitive to duty cycle value and other circuit parameters as seen in figure 3.6. Since the MMVR implies adding an inductor between flying capacitors in the SCC and output capacitor, the internal duty cycles

of SCC should be kept at their optimum values. However, as long as the value of the inductor is small, which is the case in fully integrated voltage regulators, the sensitivity of V_f to D will be small and a small mismatch in D may be acceptable and not affecting the MMVR performance so much.

As discussed previously, when duty cycle is not equal to its optimum value, the average voltage on the flying capacitor deviates from its normal value and becomes dependent on different circuit parameters causing some performance degradation. Each conversion ratio has a certain optimum duty cycle that makes the voltage on the flying capacitor balance at its normal value and becomes insensitive to other circuit parameters. In this case, the flying capacitor is considered to be stable. For the simple 2:1 topology shown in figure 3.5(a), the optimum duty cycle is half. However, the optimum duty cycle value is dependent on the SCC topology and its configuration when providing the two phases of a certain conversion ratio. Therefore, other conversion ratios or topologies may have optimum duty cycles that are not necessarily equal to half. To ensure more stability for the flying capacitor, the internal duty cycle should be as close as to the optimum duty cycle for that conversion ratio.

3.4 Analysis and Comparison

In this section, the performance of the proposed voltage regulator is discussed. We will also see how the proposed voltage regulator offers a place for better performance than both main types of voltage regulators easing the integration of voltage regulators on chip. We will revisit the main issues for each regulator type mentioned in chapter 1 and see how the proposed voltage regulator worked on solving these issues and reducing the gap between both types of voltage regulators. Since the proposed voltage regulator is a hybrid voltage regulator structure,

its performance analysis is studied from the point of view of each type of voltage regulators.

3.4.1 Comparison with Inductor-based Voltage Regulators

Starting with the buck converter, the main limitation factor or concern is the inductor size which is an obstacle in integrating it on chip especially when large inductor sizes are required. In the MMVR, the inductor size can be reduced beyond that of buck converters by just increasing the number of voltage levels provided by the SCC. Recalling the inductor ripples relation defined in previous chapter, the worst case peak-to-peak inductor current ripples $\Delta i_{L,p-p}$ that may happen inside any operation region of MMVR is given by:

$$\Delta i_{L,p-p} = \frac{\Delta V}{4LF_{sw}} \tag{3.8}$$

Where ΔV represents the voltage difference between the two voltage levels of the waveform generated at the input of the inductor. In MMVR, ΔV is equal to the voltage difference between the two voltage levels of a certain operation region of the regulator. If the voltage levels are equally spaced, then the ΔV is the same for all operation regions. However, if the voltage levels are not equally spaced, the worst case ΔV that determines the worst case inductor ripples is chosen. Therefore, according to equation 3.8, the proposed voltage regulator offers lower ΔV at the inductor input allowing for smaller inductor ripples.

Figure 3.7 shows the relation between the inductor peak-to-peak current ripples (normalized to maximum ripples) and the output voltage for different number of voltage levels (n) assuming that the voltage levels the SCC is providing are equally spaced. Actually for a number of voltage levels equal to three, the circuit reduces to the 3-level buck converter discussed previously in chapter 1. Further decrease

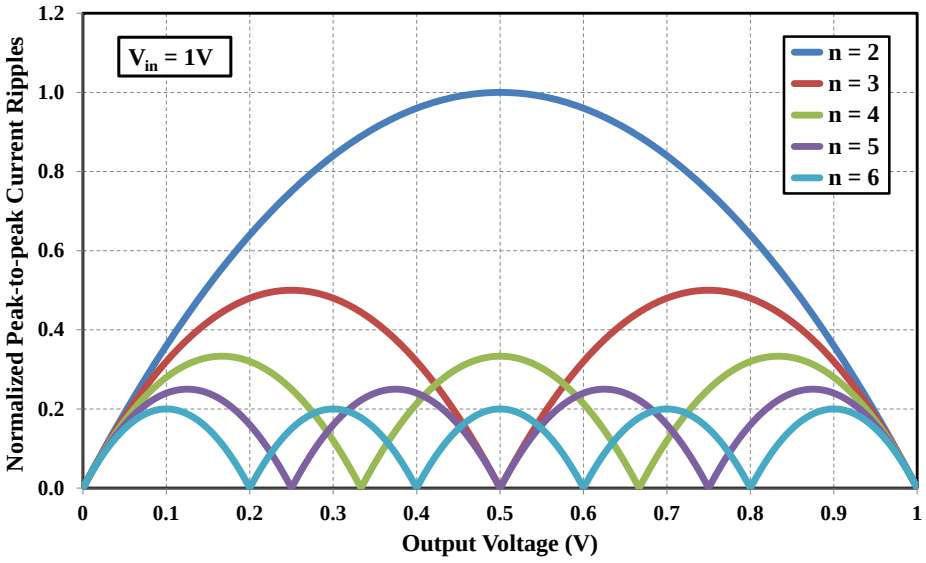


FIGURE 3.7: Inductor peak-to-peak current ripples versus output voltage for different number of voltage levels (n)

of inductor size, beyond that of 3-level buck converter, can be achieved under the proposed voltage regulator by increasing number of voltage levels available from SCC.

Increasing the number of voltage levels available from SCC gives an optimization space that can be used to either reduce the inductor size while keeping the inductor ripples the same or decrease the inductor ripples using the same inductor size. Figure 3.8 shows the relation between the inductor size and the number of voltage levels for same inductor ripples. It is interesting to note that increasing the number of voltage levels available from the SCC after a certain amount would have little effect on the inductor size. So, to sum up, the inductor size can be reduced to an extent that makes it suitable for efficient integration on chip just by controlling the number of voltage levels the SCC is providing.

Depending on the inductor characterizations of a certain technology, the preferred number of voltage levels the SCC should provide can be determined. An optimization or design procedure can be carried out as follows: a target inductor ripples are specified, then the inductor characteristics of a certain technology are

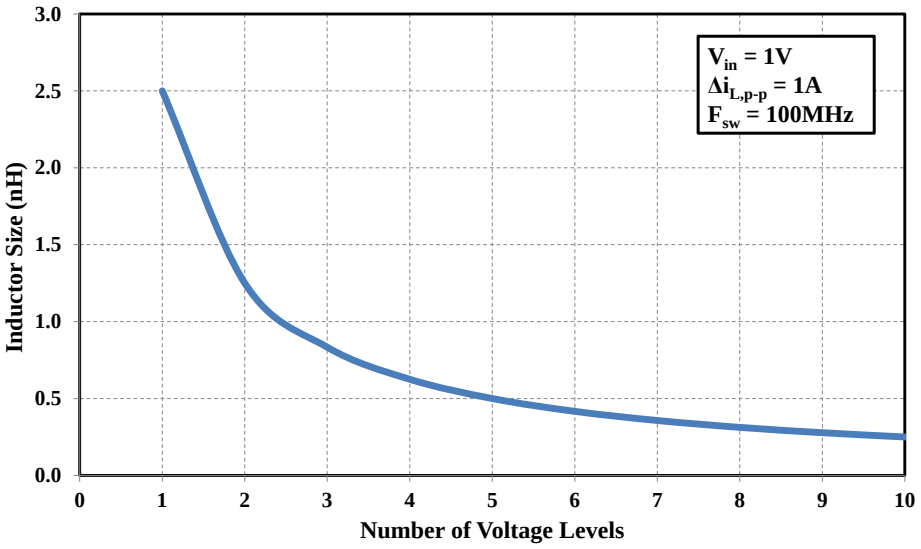


FIGURE 3.8: Inductor size versus number of voltage levels

investigated. After that, the number of required voltage levels can be determined accordingly to meet the specified target performance. We may need to go into several iterations of this process until the optimum performance is achieved.

On the other hand, we should put into consideration that increasing number of voltage levels may involve adding more components (caps and switches), each with its associated parasitics, which will degrade the performance in general. Therefore, there is a balance to be made between the inductor characteristics a certain technology is providing and the number of voltage levels required from the SCC topology in order to get the optimum performance. In other words, if the technology is providing an inductor with poor characteristics, we have to go with the option of increasing number of voltage levels in order to use a smaller inductor and compensate for the losses induced by the inductor.

Theoretically, from on-chip integration aspect, the MMVR exhibits higher performance in terms of efficiency and output voltage ripples compared to conventional buck converter. This is mainly because it offers reduced current ripples for the same inductor size compared to conventional buck converter.

3.4.2 Comparison with Capacitor-based Voltage Regulators

Looking at the proposed voltage regulator from the point of view of switched capacitor VRs, the main limiting factor in switched capacitor VRs was charge sharing losses between flying capacitors and output capacitor. In the proposed MMVR, there is an inductor between the flying capacitors and the output capacitor that works on restoring some of these inherent losses. Depending on the size of the inductor used, the SSL losses is reduced or even eliminated.

The second limiting factor of capacitor-based VRs is the lossy regulation scheme where the switching frequency is the main control parameter for the output voltage. In the proposed MMVR, the main controlling parameter for output regulation is a duty cycle (i.e. PWM regulation scheme), so the performance does not degrade quickly when deviating from target operation points. This is because the power loss of the regulator is not highly dependent on duty cycle as it is for switching frequency. From the regulation point of view, the MMVR is working mainly as a buck converter instead of a switched capacitor VR where the controlling techniques are well studied and optimized.

Access to different output voltage ranges with high efficiency is another concern in normal switched capacitor VRs where it is limited by the number of conversion ratios provided by the switched capacitor topology. To access more regions with high efficiency, additional conversion ratios have to be added which may involve adding more capacitors and switches. This degrades the performance of the switched capacitor voltage regulator in general. On the other hand, in the proposed MMVR, the whole range of output voltage is accessible starting from input voltage down to zero through different operation regions as discussed previously. Assuming that all voltage levels are equally spaced, the efficiency of the voltage regulator during each operation region is theoretically identical in terms of RMS value of inductor current ripples as indicated by figure 3.7. The peak RMS value

occurs at the middle of each operation region (when main duty cycle is equal to 0.5). This means that for higher number of voltage levels, the MMVR should experience an almost flat efficiency (i.e. constant losses) with respect to output voltage.

3.5 Summary and Conclusion

The MMVR offers several opportunities for solving challenges related to integrated voltage regulators by introducing a new set of voltage regulators suitable for that purpose. The analysis of the proposed voltage regulator shows significant performance improvements compared to current existing voltage regulators. Table 3.2 summarizes the different solutions the MMVR is providing to the issues of both voltage regulator types discussed in the previous chapter.

Many specific voltage regulators can be built based on the proposed general structure of the voltage regulator where The SCC block can be established using any of the known switched capacitor circuit topologies or using new topologies developed based on the proposed concepts. The LPF can be sized accordingly based on the SCC topology selected to ensure optimum performance of the voltage regulator. Each specific voltage regulator can suit a certain application under a given technology.

TABLE 3.2: Summary of solutions provided by MMVR for issues related to both voltage regulator types

Issue		MMVR Solution
Inductor-based Voltage Regulators	Large Inductor	Inductor size can be reduced by increasing number of voltage levels the SCC is providing
	Dynamic response	Faster dynamic response due to smaller inductor
Capacitor-based Voltage Regulators	Inherent losses due to charge sharing between flying and output capacitors	The inductor between flying and output capacitors eliminates these losses
	Lossy regulation scheme using switching frequency	Efficient regulation scheme using PWM techniques
	Access to wide output range that may require additional conversion ratios	Access to the whole operation range starting from V_{in} down to zero is available through different operation regions

Chapter 4

Phase Interleaving Technique

4.1 Introduction

In this chapter, a controlling technique that results in a further boost in the performance of the multilevel multistate voltage regulator has been proposed. It is a technique to operate the regulator different than the regular way described in the previous chapter. In this technique, the phases of the two voltage levels, the output of the SCC is switching between, are interleaved. For simplicity, the following discussion of phase interleaving technique in this chapter is assuming that the SCC is working at a certain operation region where each voltage level is provided by two phases and that the inner duty cycles of these two voltage levels are half. When the MMVR is operating in a certain operation region in its regular way, the voltage level one is provided with its two phases following the voltage level two with its two phases as shown in figure 4.1. Under the phase interleaving technique, the first phase of the first voltage level is followed by the first phase of the second voltage level, then comes the second phase of the first voltage level followed by the second phase of the second voltage level as shown in figure 4.1. Therefore, the phases of the two voltage levels are interleaved.

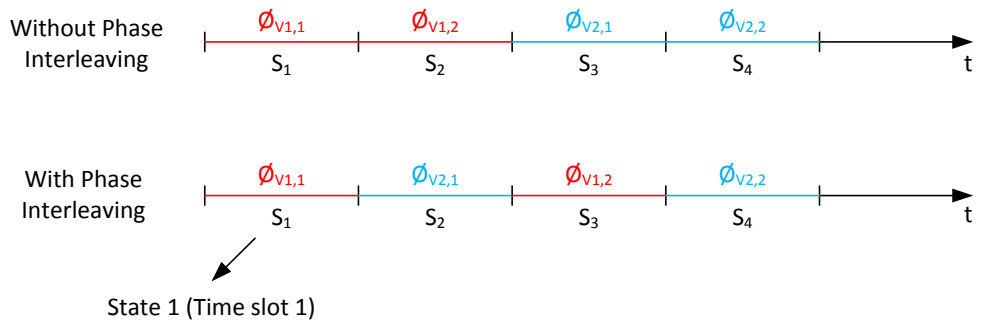


FIGURE 4.1: Operation timeline of MMVR with and without phase interleaving technique

The phase interleaving technique (PIT) works on enhancing the switching behavior of the MMVR by increasing its effective switching frequency without or with minimal overhead cost. Since the phase interleaving technique is actually a controlling technique, the physical structure of the MMVR as well as the conditions for proper operation of the regulator (e.g. the flying capacitor stability) discussed in the previous chapter are still the same.

Figure 4.2 shows the operation timeline of MMVR in a certain operation region as the main duty cycle goes from one down to zero. It is interesting to note that the phase interleaving technique has its maximum effect on the circuit performance when D = 0.5. As the main duty cycle approaches zero or one (i.e. at the edges of the operation region), the operation timeline approaches that of a MMVR operating without phase interleaving technique and in this case the phase interleaving technique advantage on the circuit performance is minimized.

When operating the regulator with the phase interleaving technique, each component in the regulator will experience its own effective switching frequency. Therefore, it is better to study the effect of applying this technique with respect to each component separately. These components are the charge-transferring components which include the inductor, the flying capacitors and the switches. Recalling

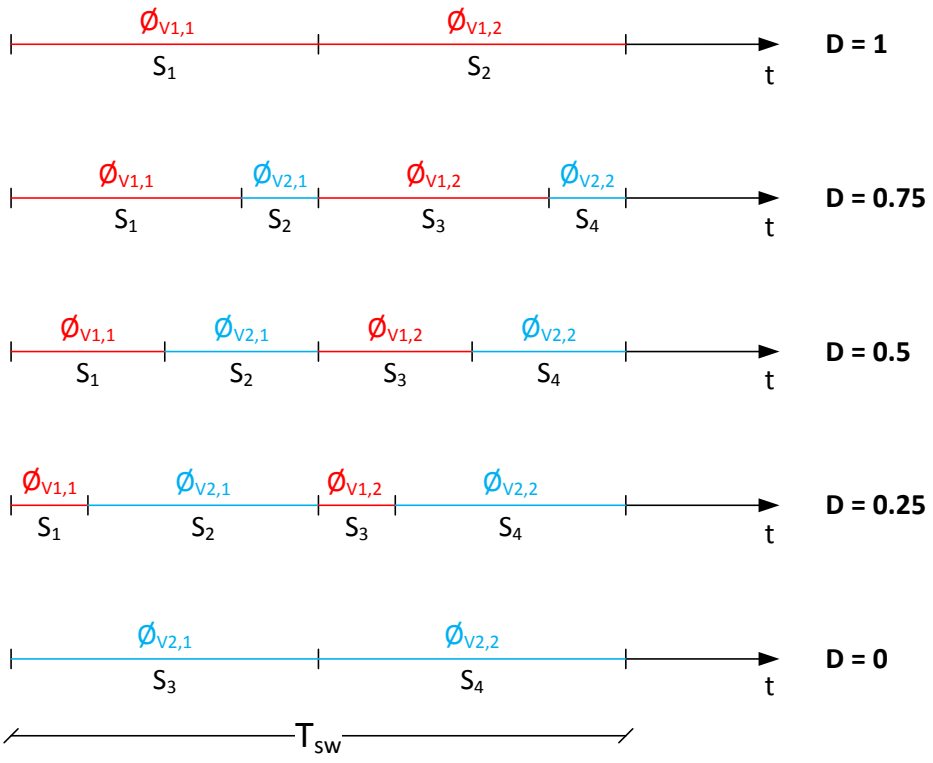


FIGURE 4.2: Operation timeline under phase interleaving technique when Main Duty Cycle (D) goes form 1 down to 0

the definition of the main switching frequency of the regulator defined in the previous chapter, and generally speaking, the effective switching frequency for each component may be higher than, less than or equal to the main switching frequency of the regulator. In the following part, the relation between the effective switching frequency for each component and the general switching frequency of the regulator is defined. This study will also help to gain more knowledge about the performance of MMVR under the phase interleaving technique and in general.

4.2 Inductor Effective Switching Frequency

Starting with the inductor, the main quantity we care about is its current ripples given before in equation 3.8. In this section, we are going to compare between

inductor worst case peak-to-peak current ripples of the MMVR with and without phase interleaving technique. After applying the phase interleaving technique, the effective switching frequency of the inductor becomes different than main switching frequency of regulator. In this case, the peak-to-peak value of inductor current ripples becomes a function in the effective switching frequency of the inductor not the main switching frequency. Generally, the effective switching frequency seen by the inductor ($F_{sw,eff,L}$) is given by:

$$F_{sw,eff,L} = n_L F_{sw} \quad , n_L \geq 1 \tag{4.1}$$

Where n_L is a factor representing the boost in the effective switching frequency of the inductor and F_{sw} is the main switching frequency of the MMVR and is equal to one over the period of one switching cycle. In this case, the new value of inductor peak-to-peak current ripples is given by:

$$\Delta i_{L,p-p} = \frac{\Delta V}{4LF_{sw,eff,L}} = \frac{\Delta V}{4Ln_L F_{sw}} \tag{4.2}$$

Equation 4.1 shows that the effective switching frequency is boosted by a factor of n_L. Note that n_L factor is always greater than or equal to one where (n_L=1) means the phase interleaving technique is not applied. This indicates that the phase interleaving technique always results in a boost in the effective switching frequency of the inductor. This, in turn, results in smaller current ripples (as depicted in equation 4.2) which means smaller RMS value of inductor current and hence smaller conduction losses. Figure 4.3 shows inductor ripples with and without phase interleaving technique. For a SCC switching its output between two voltage levels V1 and V2 each with internal duty cycle of half, n_L is equal to two which means that the effective switching frequency of the inductor is doubled when using this controlling technique (as appears in figure 4.3).

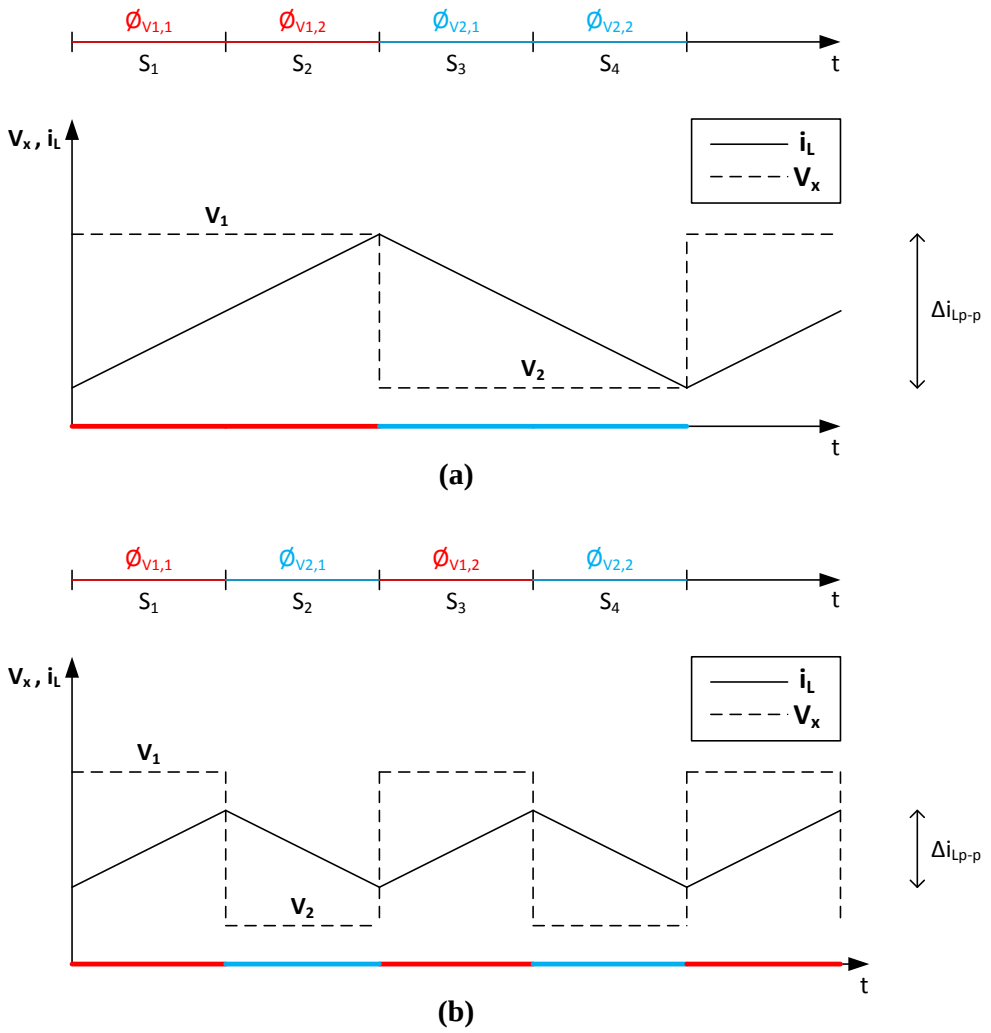


FIGURE 4.3: Inductor current ripples and SCC output waveform (a) before and (b) after applying phase interleaving technique

The previous discussion assumes that the internal duty cycles of the two voltage levels are half. However, when the internal duty cycles are not half, the effective switching frequency of the inductor and hence the peak-to-peak value of inductor current ripples becomes a function in internal duty cycles as well. In this case, each operation region may have its different n_L value depending on the internal duty cycles of the two voltage levels of that operation region. Recalling that the worst case peak to peak current ripples was when main duty cycle is half. This is assuming that the internal duty cycles of voltage levels are half. But generally

speaking, when the internal duty cycles are not half, the worst case inductor ripples is not necessarily at D=0.5.

4.3 Capacitor Effective Switching Frequency

The phase interleaving technique has an impact on two important aspects related to flying capacitors or charge transferring capacitors which are the voltage ripples on the flying capacitor (ΔV_f) and the switching losses related to the bottom plate parasitic of the flying capacitor. These aspects in turn have a considerable impact on the performance of the MMVR.

4.3.1 Flying Capacitor Voltage Ripples

Starting with the voltage ripples on the flying capacitor, these ripples results from the charging/discharging behavior of the flying capacitor in different phases. The peak-to-peak voltage ripples ΔV_f on a flying cap (C_f), generally speaking, is given by:

$$\Delta V_f = \frac{I_L}{2C_F F_{sw,eff,Cf}} \tag{4.3}$$

Where I_L is the average load current drawn from the flying capacitor, and $F_{sw,eff,Cf}$ is the effective switching frequency of the flying capacitor. This is assuming that the duty cycle is equal to half which means that the charging time is equal to the discharging time for the flying capacitor. Once the duty cycle deviates from half, the ΔV_f starts to increase. The ΔV_f on flying caps results in non-constant output voltage levels from the SCC. The effect of having ΔV_f on caps is similar to the effect of having a varying input voltage in a conventional buck converter. This is translated to higher peak-to-peak current ripples in the inductor. Higher inductor

ripples means higher RMS value for the current in the inductor and hence higher conduction losses.

Assuming that we have a SCC switching its output between two voltage levels each provided by two phases and assuming that the two voltage levels have half internal duty cycles. Generally, for each voltage level provided by two phases, when one flying capacitor is charging in one phase, it should be discharging in the next phase so that this flying capacitor is balanced at a certain value. In the following discussion, the worst case ΔV_f that may happen in a certain operation region for a MMVR operating with and without phase interleaving technique are illustrated. This is done by investigating the operation timeline of the MMVR when working inside a certain operation region to see what happens exactly to the ΔV_f on a flying cap.

Without phase interleaving technique, the first voltage level comes with its two phases where the flying cap is charging in the first phase and discharging in the second one, then similarly comes the second voltage level with its two phases where the same flying capacitor is charging in one phase then discharging in the second phase. Actually, the ΔV_f on the flying capacitor is a function in the main duty cycle value. The least ΔV_f on a flying capacitor is obtained when D = 0.5. The ΔV_f on C_f starts to increase as D deviates from half where the worst case ΔV_f happens when D = 0 or 1, as shown in figure 4.4(a), which means the MMVR is working at the edges of the operation region where only one voltage level is provided.

With the phase interleaving technique, the first voltage level comes with its first phase where the flying capacitor is charging, then comes the second voltage level with it first phase where the flying capacitor is still charging. After that comes the second phase of the first voltage level and the second phase of the second voltage level where the flying cap is discharging in both of them. Figure 4.4(b) shows the voltage on the flying capacitor (V_f) at D = 0.5 (i.e. at middle of operation region)

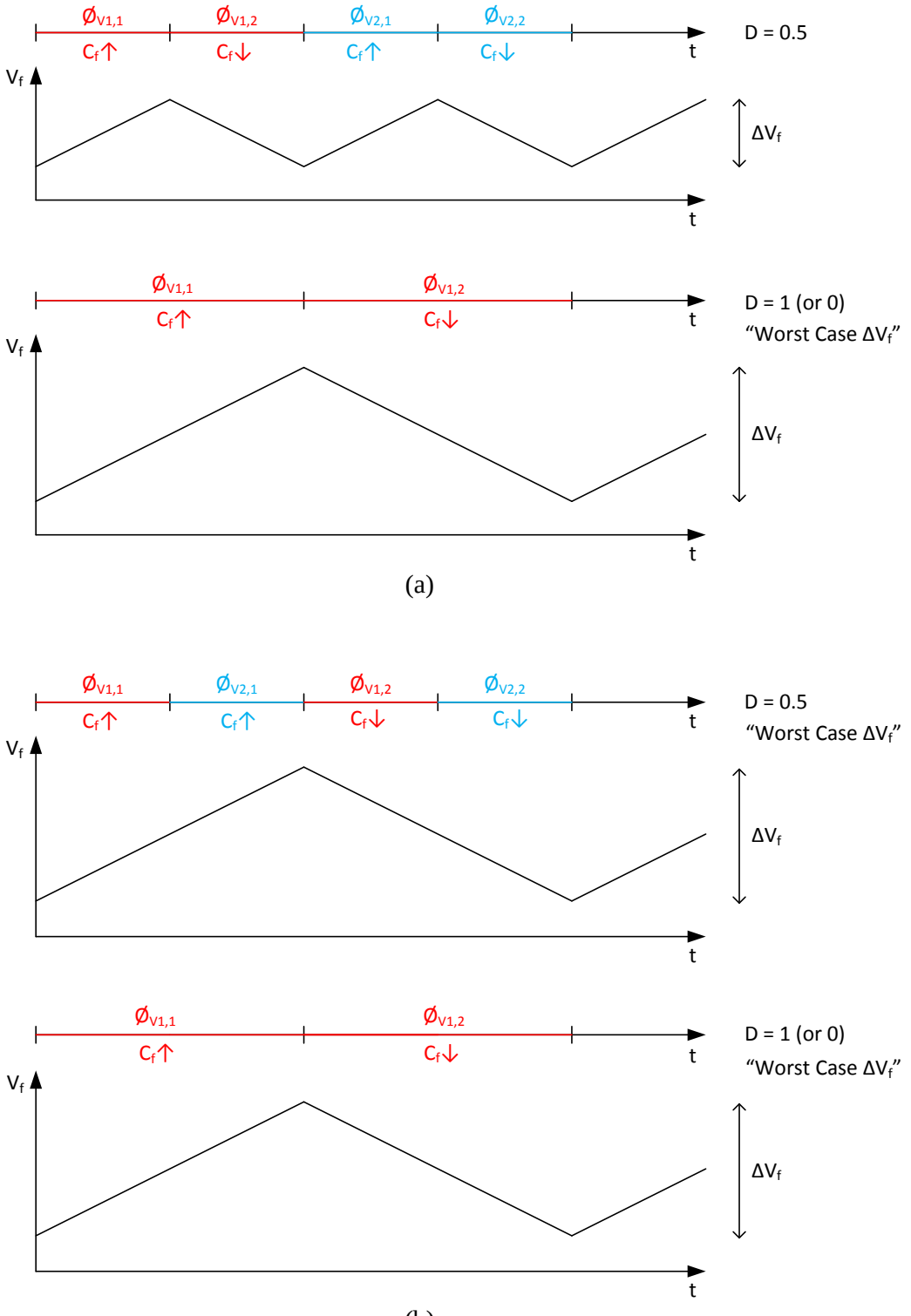


FIGURE 4.4: Flying capacitor voltage ripples (a) before and (b) after applying phase interleaving technique

and when D = 0 or 1 (i.e. at edges of operation region). We can see that the ΔV_f on the flying cap remains constant as D goes from 0.5 to 0 or 1 and that the worst case ΔV_f on the flying caps in this case is the same during the whole operation region.

It is important to note that the worst case ΔV_f on flying capacitors is not affected after applying the phase interleaving technique. The only difference is in the point at which the maximum ΔV_f occurs in terms of the duty cycle value according to figures 4.4(a) and 4.4(b). With the phase interleaving technique, the maximum occurs when D = 0.5. Without phase interleaving technique, the maximum occurs when D = 0 or 1. The maximum ΔV_f on flying capacitors is still the same in both cases which means n_c is equal to one. This is for a special case where the voltage level is provided by two phases only which is the case in most of switched capacitor topologies. The phase interleaving technique may result in higher effective switching frequency (i.e. lower ΔV_f) for SCC topologies where each voltage level is provided by more than two phases.

4.3.2 Flying Capacitor Switching Losses

The second quantity related the flying cap and affecting the performance is the switching losses due to the bottom plate capacitance which is a parasitic capacitance connected between the flying capacitor negative terminal and the ground. This bottom plate capacitance is being charged/discharged during the switching behavior of the circuit causing switching losses.

When going from one phase to another, the negative terminal of the flying capacitor may change its connection to a node of different voltage than the one in the first phase as shown in 4.5. Hence, the bottom plate parasitics of the flying capacitor experiences two different voltages in the two phases. The ΔV between

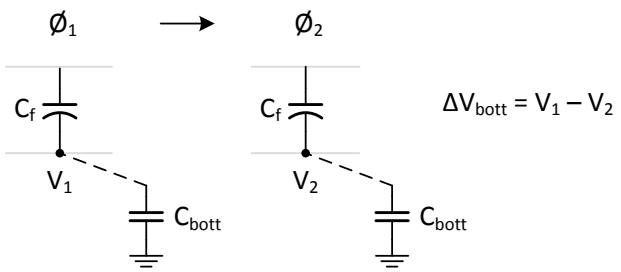


FIGURE 4.5: Voltage difference on bottom plate capacitance when going from one phase to another

these two voltage values represents the charge dissipated from the bottom-plate capacitance due to this transition between the two phases.

The sum of these voltage differences during a one complete switching cycle (i.e. four transitions) represents the total losses exhibited by the bottom plate parasitic capacitance in one switching cycle. This quantity can be used as a factor to represent switching losses due to bottom-plate capacitance and is given by:

$$\Delta V_{bott,t} = \sum_{i=1}^{k} |\Delta V_{bott,i}| = |\Delta V_{bott,1}| + |\Delta V_{bott,2}| + |\Delta V_{bott,3}| + |\Delta V_{bott,4}| \qquad (4.4)$$

where k represents number of transitions in one switching cycle (which is equal to four in case of two voltage levels each with two phases). In this case, the total switching losses due to bottom plate capacitance ($P_{loss,bottom}$) is given by:

$$P_{loss,bottom} = (\Delta V_{bott,t})^2 C_{bott} F_{sw} \qquad (4.5)$$

where C_{bott} is the bottom plate capacitance of the flying capacitor and F_{sw} is the frequency of one switching cycle.

Since the $\Delta V_{bott,t}$ for a flying capacitor is dependent on the topology as well as the switching sequence between phases, it is difficult to get a general conclusion on the effect of the phase interleaving technique on bottom-plate parasitic losses. Generally, there will be a difference in total bottom plate losses before and after applying the phase interleaving technique because the sequence of phases is different and this difference is dependent on the SCC topology used.

4.4 Switch Effective Switching Frequency

The effective switching frequency of a switch is directly related to the switching losses. The lower the effective switching frequency, the lower the switching losses. Generally, the MOSFET switching loss ($P_{loss,switch}$) arises from its gate capacitance being charged/discharged when it turns on and off, and is given by:

$$P_{loss,switch} = V_{sw}^2 W_{sw} C_{gate} F_{sw} \tag{4.6}$$

Where V_{sw} is the voltage swing on the gate capacitance during turning on and off, W_{sw} is the MOSFET width, C_{gate} is the gate capacitance of the MOSFET per unit width (F/m) and F_{sw} is the switching frequency. Any SCC topology contains a group of switches used for changing its configuration when going from one phase to another. Hence, when going from one phase to another, some of these switches are being turned on, some are being turned off and some stay in their previous state as illustrated in figure 4.6. Switches that do not change there status should not be included in the power loss calculation. Assuming that all switches have the same characteristics (i.e. same W_{sw} and same C_{gate}) and assuming that a full voltage swing occurs at the gate of each MOSFET at each transition, the total power loss due to switching Mosfets $P_{loss,switches}$ in one switching cycle is given by:

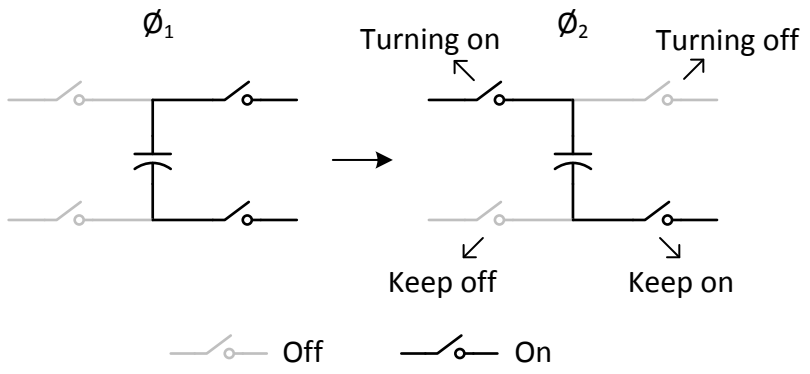


FIGURE 4.6: An example on a SCC changing its configuration

$$P_{loss,switches} = V_{sw}^2 W_{sw} C_{gate} F_{sw,eff,switches} \tag{4.7}$$

where $F_{sw,eff,switches}$ is the total effective switching frequency of MOSFETs for one switching cycle and is given by:

$$F_{sw,eff,switches} = \frac{1}{2} n_s F_{sw} \tag{4.8}$$

where n_s represents the total number of MOSFET switchings in one switching cycle and F_{sw} is the frequency of one switchng cycle.

The total number of switchings means the sum of the number of switches being turned on or off when going from one state to another for a full switching cycle. It is divided by two because the number of switchings n_s includes both switching on and off of switches. The n_s factor can be used as a metric to compare between the total MOSFET switching loss of different SCC topologies operating with certain phase sequences. The lower the number of switching MOSFETs , the lower the effective switching frequency of switches and hence the lower the MOSFET switching losses.

In our example case study, the full switching cycle consists of four states, hence n_s means the total number of MOSFET switchings when going from state one to state two and so on for all the four states then going back to state one again; this represents the total number of MOSFET switchings in one cycle. To know the effect of the phase interleaving technique on the MOSFET switching losses in the MMVR, we can compare between the n_s value before and after applying the phase interleaving technique. Once again,it is difficult to put a general rule whether the PIT results in a reduced number of switching MOSFETs or not because this is dependent on the topology structure as well as the phase sequence in one switching cycle. However, in most cases, the PIT results in less number of branches changing their states and hence in lower number of switching MOSFETs.

4.5 Summary and Conclusion

Generally speaking and based on the previous discussion, the phase interleaving technique can result in several enhancements in the switching behavior of the regulator. These enhancements are maximized when operating at the middle of a certain operation region (i.e. when main duty cycle is near 0.5) while at the edges of an operation region, the phase interleaving effect is not significant because almost only one voltage level is present. The effect of the phase interleaving technique on the MMVR performance may differ from one operation region to another because the phase sequence in each operation region is different. The performance boost due to phase interleaving technique may be more significant in certain operation regions than others.

In previous sections, some metrics to measure the effect of the phase interleaving technique on the MMVR have been defined. Based on these metrics, we can decide whether to use the phase interleaving technique or to use the general switching

technique. Although, the phase interleaving technique always offers better effective switching frequency for inductors, which is the main concern in integrated voltage regulators, the effective switching frequency for capacitors and switches are still dependent on the topology. Table 4.1 summarizes the effect of the phase interleaving technique on the MMVR.

The analysis done in this chapter was for the case of two voltage levels each with two phases. For SCC with voltage levels provided by more than two phases, the phase interleaving technique can result in a performance boost too, but it is beyond the scope of this work discuss that. From the above discussion, we can see that the phase interleaving technique offers a chance to boost the performance of the proposed MMVR. This can be well illustrated in the design example in the next chapter.

TABLE 4.1: Summary of phase interleaving technique effect on MMVR performance

Parameter		Effect
Effective switching frequency of inductors		Increased allowing for smaller inductor sizes
Capacitor	Worst case ΔV_f	The same (not affected)
	Bottom plate parasitics	Dependent on SCC topology and phase sequence
Effective switching frequency of switches		Dependent on SCC topology and phase sequence but most likely decrease

Chapter 5

4-Level 4-State Voltage Regulator

5.1 Introduction

The general structure of the proposed MMVR as well as some techniques and methods for operating the MMVR have been introduced in the previous two chapters. Many voltage regulator circuit designs or implementations targeting different applications can be built based on the aforementioned principles and techniques. Several SCC topologies exist in the literature [24, 34–36] which can be used in the SCC block to build the full circuit of the MMVR. Each SCC topology, when used under the MMVR technique, will offer a behavior that is completely different form its behavior when used as a conventional switched capacitor voltage regulator. Each SCC topology offers a certain number of voltage levels and states that may be suitable for certain technologies and applications. In other words, for a given technology and a given target application, a certain SCC topology may offer the optimum performance compared to other SCC topologies.

In this chapter, the conventional known triple-ratio SCC topology (or series-parallel topology) is selected to build a MMVR circuit where all rules and techniques discussed in the previous two chapters are applied. The resulted circuit

is called a 4-level 4-state voltage regulator. In the following sections, the circuit structure of the 4-level 4-state voltage regulator is discussed. Then, some analysis on the VR circuit is done. After that, two implementations of the 4-level 4-state VR on CMOS standard technology are provided along with performance comparisons with other existing VRs.

5.2 Circuit Structure and Operation

5.2.1 Circuit Structure

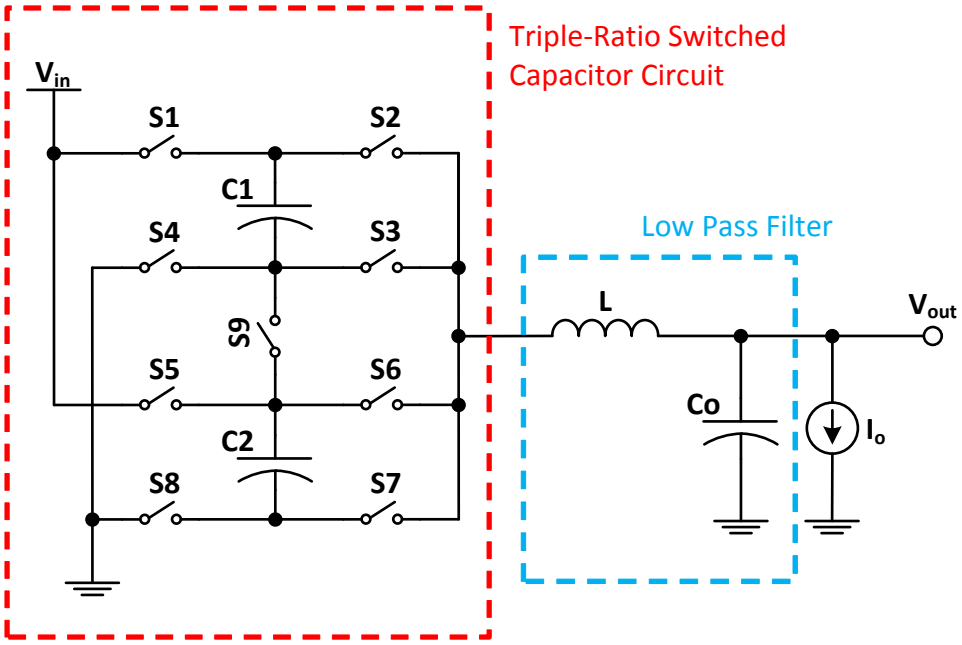


FIGURE 5.1: 4-Level 4-State voltage regulator

Figure 5.1 shows the general structure of the 4-level 4-state voltage regulator. It consists of series-parallel SC topology followed by a LPF. The SCC topology consists of two flying caps and nine switches and is capable of providing four

voltage levels at its output including the two power supply rails (i.e. input voltage and ground). These voltage levels are:

- **'V_{in}' level**: provided by direct connection between input node and output node of the SCC (no flying caps are involved)
- **'$\frac{2}{3}V_{in}$' level**: Provided by two phases from the SCC (the two flying caps are involved)
- **'$\frac{1}{3}V_{in}$' level**: Provided by two phases from the SCC (the two flying caps are involved)
- **'Gnd' level**: provided by direct connection between ground node and output node of the SCC (no flying caps are involved)

The SCC configurations that generate the four voltage levels are provided in table 5.1. The table shows the status of all switches and flying capacitor in each phase. The up-arrow means the flying capacitor is charging in that phase while the down-arrow means the flying capacitor is discharging. Note that the 'V_{in}' and 'Gnd' voltage levels are provided by one phase only (i.e. one SCC configuration) because there are no flying caps involved in the charge transferring process. On the other hand, the other two voltage levels $\frac{2}{3}V_{in}$ and $\frac{1}{3}V_{in}$ are provided by two phases because the two flying caps are involved in the the charge transferring process where in one phase the flying caps are charging/discharging then in the next phase the flying caps are discharging/charging so that they can balance at a certain voltage. In this SCC topology, the two flying caps are normally balanced at $\frac{1}{3}V_{in}$. This comes from the nature of the connections of the two flying caps in the two phases of each voltage level.

Although the same topology is capable of providing 2:1 conversion ratio (i.e. $\frac{1}{2}V_{in}$ voltage level), this conversion ratio is excluded because it is not satisfying the conditions of the SCC aforementioned in chapter 2. In 2:1 conversion ratio, the two

TABLE 5.1: SCC configuration for different voltage levels in the 4-level 4-state VR

Switches & Capacitors	Voltage Level					
	V_{in}	$\frac{2}{3}V_{in}$		$\frac{1}{3}V_{in}$		Gnd
	ϕ_1	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1
S1	ON	ON	OFF	ON	OFF	OFF
S2	ON	OFF	ON	OFF	ON	OFF
S3	OFF	ON	OFF	OFF	OFF	OFF
S4	OFF	OFF	OFF	OFF	ON	ON
S5	ON	ON	OFF	OFF	OFF	OFF
S6	OFF	OFF	OFF	OFF	ON	OFF
S7	OFF	ON	OFF	ON	OFF	ON
S8	OFF	OFF	ON	OFF	OFF	ON
S9	OFF	OFF	ON	ON	OFF	OFF
C1	–	↑	↓	↑	↓	–
C2	–	↑	↓	↑	↓	–

flying caps are balanced at half input voltage while in the other two conversion ratios, they are balanced at $\frac{1}{3}V_{in}$. Hence, the condition that each flying cap is balanced at the same voltage during all conversion ratios is not satisfied. That is why the 2:1 conversion ratio has been excluded.

5.2.2 Flying Capacitor Stability

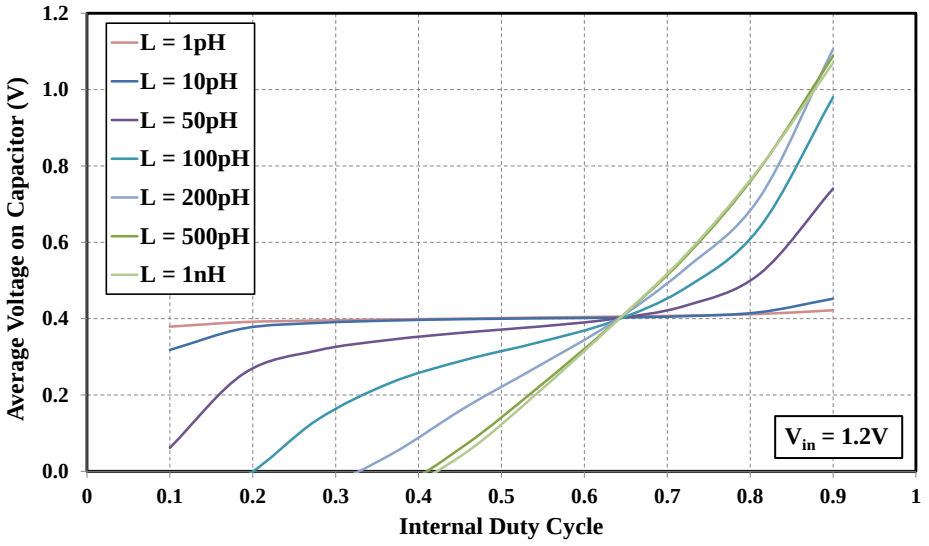
As explained previously, each voltage level has an optimum inner duty cycle (i.e. relative duration between voltage level phases) that makes each flying cap balance at its normal value which is $\frac{1}{3}V_{in}$ for the SCC topology we are using. We

have to ensure that the flying capacitors are balanced at $\frac{1}{3}V_{in}$ to ensure a reliable and constant output voltage level from the SCC topology. Because of the existence of the inductor in the path from input voltage towards output voltage, the average voltage on the flying capacitor (V_f) becomes a function in internal duty cycle of each voltage level. Figure 5.2(a) and 5.2(b) show that the optimum inner duty cycle for voltage levels $\frac{2}{3}V_{in}$ and $\frac{1}{3}V_{in}$ are $\frac{2}{3}$ and $\frac{1}{3}$ respectively. Thus, to ensure the flying capacitors are balanced at their normal values (i.e. $\frac{1}{3}V_{in}$), the optimum relative duration between two phases of each of these two voltage levels should be satisfied. Moreover, at the optimum internal duty cycle values, the average voltage on the flying capacitors becomes independent of inductance value as shown in figure 5.2(a). This ensures more stability in (V_f) value versus variations in circuit parameters. Note that the 'V_{in}' and 'Gnd' voltage levels have 'do not care' internal duty cycle values since they consist of two subsequent identical phases. Therefore, their internal duty cycles are assumed to be half. Table 5.2 shows the values of the internal duty cycles for the four voltage levels of the SCC.

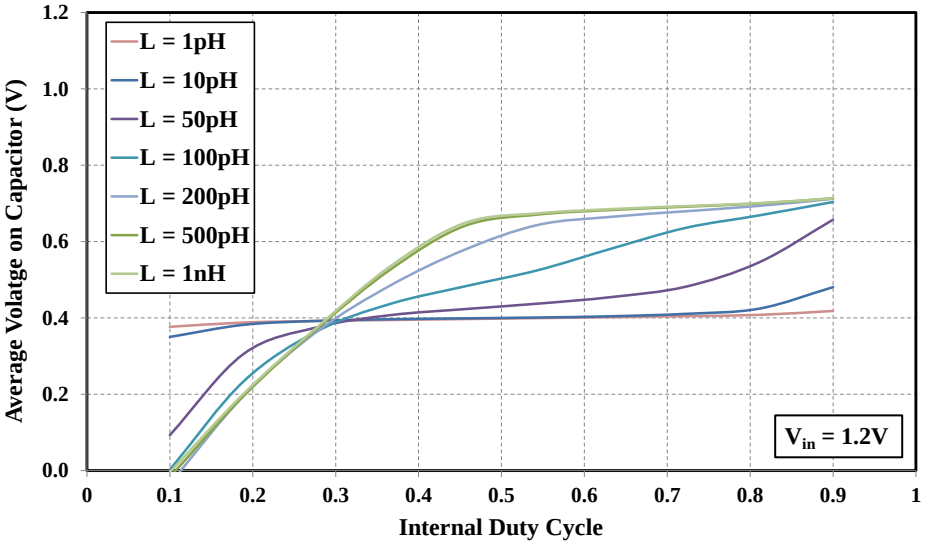
TABLE 5.2: Internal duty cycle values of each voltage level

Voltage Level	$D_{internal}$
V_{in}	$\frac{1}{2}$
$\frac{2}{3}V_{in}$	$\frac{2}{3}$
$\frac{1}{3}V_{in}$	$\frac{1}{3}$
Gnd	$\frac{1}{2}$

Actually, the values of the optimum internal duty cycles of voltage levels sometimes can be found intuitively rather than sweeping on the internal duty cycle. For example, in the '$\frac{1}{3}V_{in}$' voltage level, in the first phase the two flying capacitors are connected in parallel while in the second phase they are connected in series as shown in figure 5.3. This means that the load current being drawn from caps in the first phase is half of that of second phase. This means that the flying caps



(a)



(b)

FIGURE 5.2: Simulation for average voltage on flying capacitor versus internal duty cycle for different inductance values when the SCC is providing a voltage level of (a) '$\frac{2}{3}V_{in}$' (b) '$\frac{1}{3}V_{in}$'

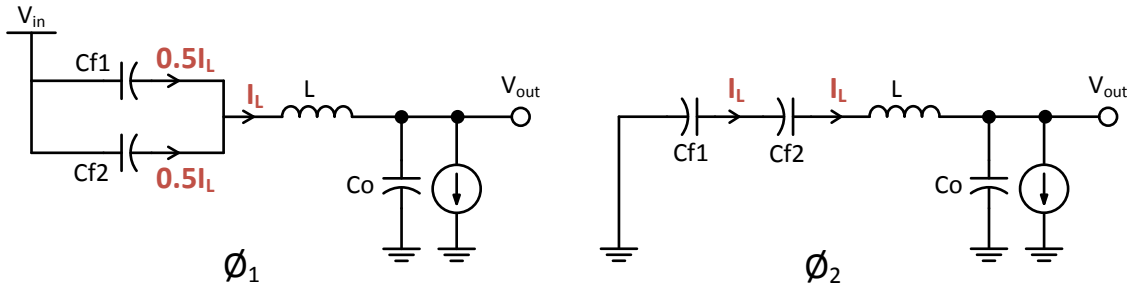


FIGURE 5.3: Two SCC configurations (phases) for '$\frac{1}{3}V_{in}$' voltage level

charging rate in the first phase is slower than the flying caps discharging rate in the second phase. Therefore, to compensate for that, the duration of the first phase is made twice the duration of the next phase which indicates an internal duty cycle of '$\frac{2}{3}$'. Similarly, this can be applied on '$\frac{1}{3}V_{in}$' voltage level and the optimum internal duty cycle can be intuitively found to be equal to '$\frac{1}{3}$'.

5.2.3 Circuit Operation

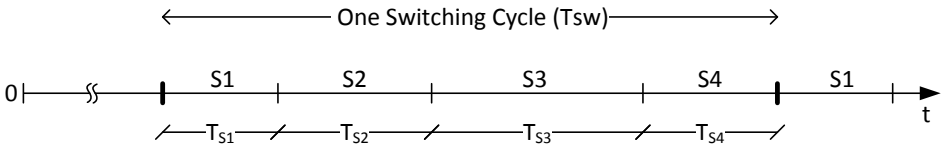


FIGURE 5.4: Operation timeline of the 4-level 4-state voltage regulator

Figure 5.4 shows the operation timeline of the circuit. A one switching cycle of the regulator is divided into four time slots called four states (hence the name 4-state regulator). Usually, in MMVR, the number of states is equal to double the maximum number of phases required to provide any voltage level which is equal to two in our case. The duration of one switching cycle is equal to one over the main switching frequency of the regulator. During regulator normal operation, this switching cycle is repeated on the operation timeline of the circuit so that the

VR produces a constant output voltage. The internal duty cycles and the main duty cycle are defined as follows

$$D1 = \frac{T_{V1,\phi1}}{T_{V1,\phi1} + T_{V1,\phi2}} = \frac{T_{V1,\phi1}}{T_{V1}} \tag{5.1}$$

$$D2 = \frac{T_{V2,\phi1}}{T_{V2,\phi1} + T_{V2,\phi2}} = \frac{T_{V2,\phi1}}{T_{V2}} \tag{5.2}$$

$$D = \frac{T_{V1}}{T_{V1} + T_{V2}} = \frac{T_{V1}}{T_{sw}} \tag{5.3}$$

where $T_{V1,\phi1}$ and $T_{V1,\phi2}$ are the duration of first and second phase of first voltage level, $T_{V2,\phi1}$ and $T_{V2,\phi2}$ are the duration of first and second phase of second voltage level and T_{V1} and T_{V2} are the total duration of first voltage level and second voltage level inside a one switching cycle respectively.

As explained in chapter 2, the SCC is configured to switch its output between two different voltage levels periodically. The four states of a switching cycle are assigned to the phases of the two voltage levels the SCC is configured to switch between. Each time slot or state has certain duration relative to the complete switching cycle duration. The duration of each state relative to the total switching cycle is defined completely by the main duty cycle (D) and the internal duty cycles (D1 and D2) as follows:

$$T_{S1} = T_{V1,\phi1} = D1 * D * T_{sw} \tag{5.4}$$

$$T_{S2} = T_{V1,\phi2} = (1 - D1) * D * T_{sw} \tag{5.5}$$

$$T_{S3} = T_{V2,\phi1} = D2 * (1 - D) * T_{sw} \tag{5.6}$$

$$T_{S4} = T_{V2,\phi2} = (1 - D2)(1 - D) * T_{sw} \tag{5.7}$$

The regulator can be configured to work at one of three different operation regions depending on the desired output voltage (V_o) value. This is for the output

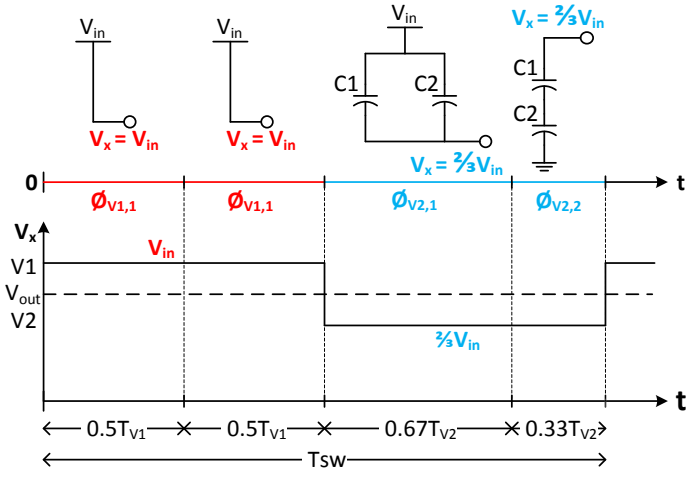
voltage coarse tuning. Figure 5.5 shows the operation timeline of the regulator in each operation region as well as the SCC output (V_x) in each time slot (the figure is to scale assuming a main duty cycle of half). The three operation regions are as follows:

1. **First operation region:** ($\frac{2}{3}V_{in} < V_o \leq V_{in}$)
   In this operation region, the SCC is configured to switch its output periodically between 'V_{in}' voltage level and '$\frac{2}{3}V_{in}$' voltage level as shown in figure 5.5(a). The internal duty cycle one (D1) of first voltage level 'V_{in}' is do not care as it consists of one phase only while the internal duty cycle two (D2) of the second voltage level '$\frac{2}{3}V_{in}$' is '$\frac{2}{3}$'.

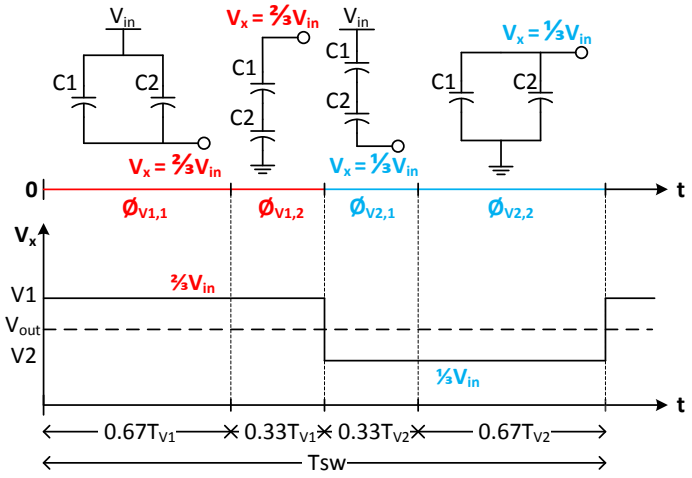
2. **Second operation region:** ($\frac{1}{3}V_{in} < V_o \leq \frac{2}{3}V_{in}$)
   In this operation region, the SCC is configured to switch its output periodically between '$\frac{2}{3}V_{in}$' voltage level and '$\frac{1}{3}V_{in}$' voltage level as shown in figure 5.5(b). The internal duty cycle one (D1) of first voltage level '$\frac{2}{3}V_{in}$' is '$\frac{2}{3}$' while the internal duty cycle two (D2) of the second voltage level '$\frac{1}{3}V_{in}$' is '$\frac{1}{3}$'.

3. **Third operation region:** ($0 < V_o \leq \frac{1}{3}V_{in}$)
   In this operation region, the SCC is configured to switch its output periodically between '$\frac{1}{3}V_{in}$' voltage level and 'Gnd' voltage level as shown in figure 5.5(c). The internal duty cycle one (D1) of first voltage level '$\frac{1}{3}V_{in}$' is '$\frac{1}{3}$' while the internal duty cycle two (D2) of the second voltage level is do not care as it consists of one phase only.

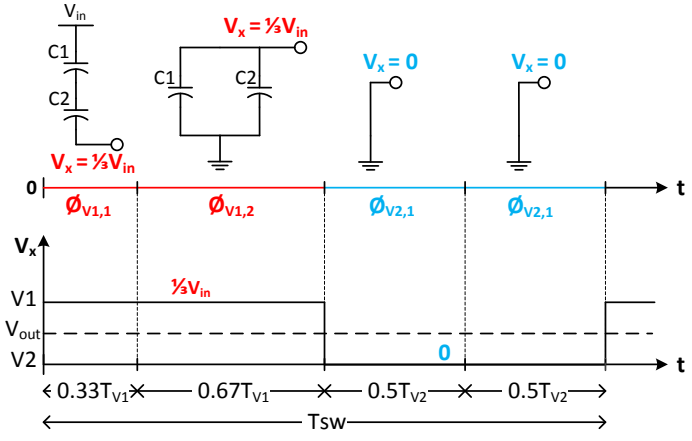
Table 5.3 summarizes the two voltage levels of each operation region and their corresponding inner duty cycles. Fine tuning of output voltage level inside each operation region is done by adjusting the main duty cycle (D) value which controls the relative duration between the two voltage levels of each operation region. When the working point is approaching the edges of a certain operation region (i.e. D



(a)



(b)



(c)

FIGURE 5.5: Operation timeline showing SCC configurations and switching voltage waveform (V_x) at (a) first, (b) second and (c) third operation regions

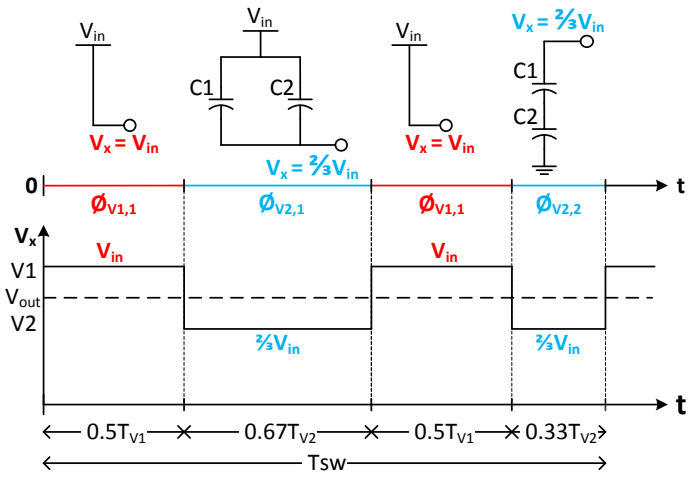
$\approx$ 1 or 0), the SCC can be configured to work at one voltage level only. It can be noted that a full access to the whole range starting from V_{in} down to zero is available through the MMVR by first selecting the appropriate operation region and then adjusting the main duty cycle inside that operation region to get the desired output voltage.

TABLE 5.3: Internal duty cycle values in each operation region

	V1	V2	D1	D2
First Operation Region	V_{in}	$\frac{2}{3}V_{in}$	$\frac{1}{2}$	$\frac{2}{3}$
Second Operation Region	$\frac{2}{3}V_{in}$	$\frac{1}{3}V_{in}$	$\frac{2}{3}$	$\frac{1}{3}$
Third Operation Region	$\frac{2}{3}V_{in}$	Zero	$\frac{1}{3}$	$\frac{1}{2}$

5.2.4 Applying Phase Interleaving Technique

As discussed in chapter 3, the phase interleaving technique results in several improvements in the performance of the MMVR. It is a way to operate the MMVR different than the conventional way discussed in previous subsection. Under this technique, the phases of the two voltage levels of each operation region are interleaved. Figure 5.6 shows the operation timeline of the circuit at different operation regions after applying the phase interleaving technique. It shows as well the SCC output waveform (V_x) in each operation region. It is important to note that the internal duty cycle of each voltage level remains unchanged after applying the technique. This means that the relative duration between the two phases of each voltage level must be kept at the optimum internal duty cycle value of that voltage level to ensure the stability of the flying caps at their normal values (i.e. $\frac{1}{3}V_{in}$). After applying the phase interleaving technique, the duration of each state (or time slot) relative to the total switching cycle as a function in the main duty cycle (D) and the internal duty cycles (D1 and D2) are as follows:



(a)

(b)

(c)

FIGURE 5.6: Operation timeline showing SCC configurations and switching voltage waveform (V_x) under phase interleaving technique at (a) first, (b) second and (c) third operation regions

$$T_{S1} = T_{V1,\phi1} = D1 * D * T_{sw} \tag{5.8}$$

$$T_{S2} = T_{V2,\phi1} = D2 * (1 - D) * T_{sw} \tag{5.9}$$

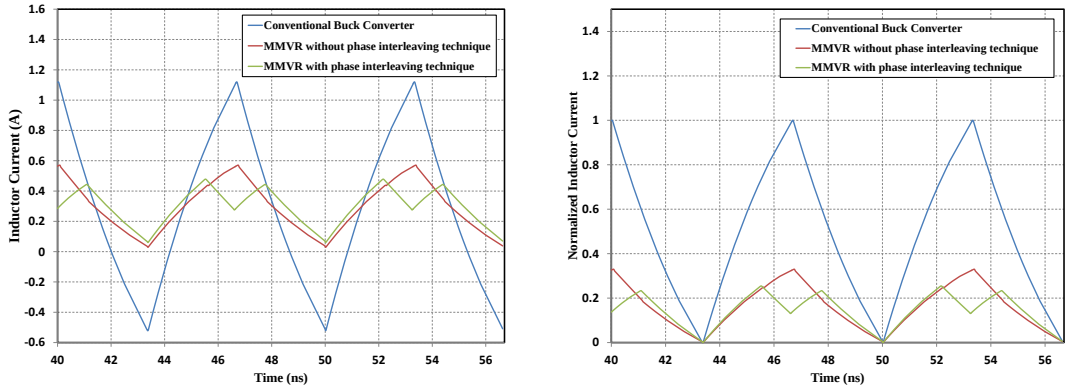
$$T_{S3} = T_{V1,\phi2} = (1 - D1) * D * T_{sw} \tag{5.10}$$

$$T_{S4} = T_{V2,\phi2} = (1 - D2)(1 - D) * T_{sw} \tag{5.11}$$

It is worth mentioning that the internal duty cycle of 'V_{in}' and 'Gnd' voltage levels in the conventional operation technique are meaningless because the two states of each of these two voltage levels are assigned to identical phases and are subsequent. However, under the phase interleaving technique, the two states of each of these two voltage levels are separated by states of the other voltage level as shown in figures 5.6(a) and 5.6(c), hence the internal duty cycles would have a meaning in this case. The values of these two internal duty cycles have minor effect on regulator's performance and are assumed to be half.

5.3 Circuit Analysis

The peak-to-peak inductor current ripples play an important role in determining the performance of the regulator. They have a direct impact on regulator's efficiency as well as regulator's output voltage ripples. Figure 5.7 shows a comparison between the peak-to-peak inductor current ripples of the MMVR when operating with and without phase interleaving technique and a conventional buck converter using SPICE simulation. The MMVR is operating in the second operation region with a main duty cycle of half while the conventional buck converter is operating with a duty cycle of half as well. Hence, both regulators are giving a same output voltage of $0.5V_{in}$. The conventional buck converter and the MMVR are operating at the same frequency and have the same inductor size. It can be noted that



(a) (b)

FIGURE 5.7: Inductor current waveform of a conventional buck converter and of a MMVR with and without phase interleaving technique with (a)absolute values and (b)normalized values to the maximum peak-to-peak current ripples

the 4-level 4-state VR offer much lower inductor ripples compared to conventional buck converter. This is mainly because the ΔV at the inductor input is equal to $\frac{1}{3}V_{in}$ for the 4-level 4-state VR while it is equal to V_{in} for the conventional buck converter. Consequently, according to equation 4.2, the inductor current ripples of the 4-level 4-state VR is one third that of conventional buck converter as shown in figure 5.7. This gives a degree of freedom to either decrease the inductor size to one third while keeping the inductor ripples the same or vice versa. This translates to performance improvement in general compared to conventional buck converter especially when there are limitations on inductor size which is the case in integrated voltage regulators.

Moreover, figure 5.7 shows that the phase interleaving technique results in a further reduction in inductor current ripples compared to a MMVR operating without phase interleaving technique. This coincides with what was predicted in chapter 4. There is an n-factor that relates the effective switching frequency of the inductor ($F_{sw,L}$) to the main switching frequency of the MMVR (F_{sw}) as discussed in section 4.2. Without phase interleaving technique, the effective switching frequency of inductor is equal to the main switching frequency of the 4-level 4-state regulator (i.e. n = 1). Under phase interleaving technique, n-factor is supposed to

equal to two if internal duty cycles of voltage levels are half as depicted in chapter 4. However, since the 4-level 4-state voltage regulator has internal duty cycles which are not necessarily equal to half, the n-factor has a different value than two. This results from the fact that the n-factor is a function in internal duty cycles as well. As shown in figure 5.7(b), the peak-to-peak inductor current ripples under the phase interleaving technique are less than that without phase interleaving technique by one third. This means that the effective switching frequency of the inductor has increased by a factor of third under the phase interleaving (i.e. n = 1.33). It can be noted that the n-factor is greater than one which means that the phase interleaving technique results in a further reduction in inductor current ripples compared to the case without phase interleaving technique.

The switching losses of the regulator has a direct relation with the number of switching MOSFETs in a one complete switching cycle. By using tables 5.4, 5.5 and 5.6, the number of switching MOSFETs (number of right arrows) in one switching cycle can be calculated for each regulator type. Table 5.7 shows a comparison between total number of switching MOSFETs for a) conventional triple-ratio switched capacitor voltage regulator, b) 4-level 4-state VR without phase interleaving technique and c) 4-level 4-state VR with phase interleaving technique. It can be noted that the 4-level 4-state VR offers a potential reduction in switching losses compared to conventional SCVR which in some cases approaches 50% reduction in number of MOSFET switchings. This opens the room for a performance improvement in the 4-level 4-state VR over the conventional SCVR. In addition, the phase interleaving technique in some operation regions results in a further reduction in MOSFET switching losses.

TABLE 5.4: SCC configuration for different operation regions in the 4-level 4-state VR operating without phase interleaving technique

Region		First Operation Region			
Time Slot		T1	T2	T3	T4
Switches Configuration	S1	ON	ON	ON →	OFF →
	S2	ON	ON →	OFF →	ON
	S3	OFF	OFF →	ON →	OFF
	S4	OFF	OFF	OFF	OFF
	S5	ON	ON	ON →	OFF →
	S6	OFF	OFF	OFF	OFF
	S7	OFF	OFF →	ON →	OFF
	S8	OFF	OFF	OFF →	ON →
	S9	OFF	OFF	OFF →	ON →
Voltage Level		V_{in}	V_{in}	$\frac{2}{3}V_{in}$	$\frac{2}{3}V_{in}$

+

Region		Second Operation Region			
Time Slot		T1	T2	T3	T4
Switches Configuration	S1	ON →	OFF →	ON →	OFF →
	S2	OFF →	ON →	OFF →	ON →
	S3	ON →	OFF	OFF	OFF →
	S4	OFF	OFF	OFF →	ON →
	S5	ON →	OFF	OFF	OFF →
	S6	OFF	OFF	OFF →	ON →
	S7	ON →	OFF →	ON →	OFF →
	S8	OFF →	ON →	OFF →	ON →
	S9	OFF →	ON	ON →	OFF
Voltage Level		$\frac{2}{3}V_{in}$	$\frac{2}{3}V_{in}$	$\frac{1}{3}V_{in}$	$\frac{1}{3}V_{in}$

Region		Third Operation Region			
Time Slot		T1	T2	T3	T4
Switches Configuration	S1	ON →	OFF	OFF	OFF →
	S2	OFF →	ON →	OFF	OFF
	S3	OFF	OFF	OFF	OFF
	S4	OFF →	ON	ON	ON →
	S5	OFF	OFF	OFF	OFF
	S6	OFF →	ON →	OFF	OFF
	S7	ON →	OFF →	ON	ON
	S8	OFF →	ON	ON	ON →
	S9	ON →	OFF	OFF	OFF →
Voltage Level		$\frac{1}{3}V_{in}$	$\frac{1}{3}V_{in}$	0	0

TABLE 5.5: SCC configuration for different operation regions in the 4-level 4-state VR operating with phase interleaving technique

Region		First Operation Region								
Time Slot		T1		T2		T3		T4		
Switches Configuration	S1	ON		ON		ON	→	OFF	→	
	S2	ON	→	OFF	→	ON		ON		
	S3	OFF	→	ON	→	OFF		OFF		
	S4	OFF		OFF		OFF		OFF		
	S5	ON		ON		ON	→	OFF	→	
	S6	OFF		OFF		OFF		OFF		
	S7	OFF	→	ON	→	OFF		OFF		
	S8	OFF		OFF		OFF	→	ON	→	
	S9	OFF		OFF		OFF	→	ON	→	
Voltage Level		V_{in}		$\frac{2}{3}V_{in}$		V_{in}		$\frac{2}{3}V_{in}$		

+

Region		Second Operation Region								
Time Slot		T1		T2		T3		T4		
Switches Configuration	S1	ON		ON	→	OFF		OFF	→	
	S2	OFF		OFF	→	ON		ON	→	
	S3	ON	→	OFF		OFF		OFF	→	
	S4	OFF		OFF		OFF	→	ON	→	
	S5	ON	→	OFF		OFF		OFF	→	
	S6	OFF		OFF		OFF	→	ON	→	
	S7	ON		ON	→	OFF		OFF	→	
	S8	OFF		OFF	→	ON		ON	→	
	S9	OFF	→	ON		ON	→	OFF		
Voltage Level		$\frac{2}{3}V_{in}$		$\frac{1}{3}V_{in}$		$\frac{2}{3}V_{in}$		$\frac{1}{3}V_{in}$		

Region		Third Operation Region								
Time Slot		T1		T2		T3		T4		
Switches Configuration	S1	ON	→	OFF		OFF		OFF	→	
	S2	OFF		OFF	→	ON	→	OFF		
	S3	OFF		OFF		OFF		OFF		
	S4	OFF	→	ON		ON		ON	→	
	S5	OFF		OFF		OFF		OFF		
	S6	OFF		OFF	→	ON	→	OFF		
	S7	ON		ON	→	OFF	→	ON		
	S8	OFF	→	ON		ON		ON	→	
	S9	ON	→	OFF		OFF		OFF	→	
Voltage Level		$\frac{1}{3}V_{in}$		0		$\frac{1}{3}V_{in}$		0		

TABLE 5.6: Switch configurations for a normal switched capacitor voltage regulator

Region		1:1 conversion ratio							
Time Slot		T1		T2		T3		T4	
Switches Configuration	S1	ON	→	OFF	→	ON	→	OFF	→
	S2	OFF	→	ON	→	OFF	→	ON	→
	S3	OFF		OFF		OFF		OFF	
	S4	ON		ON		ON		ON	
	S5	ON	→	OFF	→	ON	→	OFF	→
	S6	OFF	→	ON	→	OFF	→	ON	→
	S7	OFF		OFF		OFF		OFF	
	S8	ON		ON		ON		ON	
	S9	OFF		OFF		OFF		OFF	

+

Region		3:2 conversion ratio							
Time Slot		T1		T2		T3		T4	
Switches Configuration	S1	ON	→	OFF	→	ON	→	OFF	→
	S2	OFF	→	ON	→	OFF	→	ON	→
	S3	ON	→	OFF	→	ON	→	OFF	→
	S4	OFF		OFF		OFF		OFF	
	S5	ON	→	OFF	→	ON	→	OFF	→
	S6	OFF		OFF		OFF		OFF	
	S7	ON	→	OFF	→	ON	→	OFF	→
	S8	OFF	→	ON	→	OFF	→	ON	→
	S9	OFF	→	ON	→	OFF	→	ON	→

Region		3:1 conversion ratio							
Time Slot		T1		T2		T3		T4	
Switches Configuration	S1	ON	→	OFF	→	ON	→	OFF	→
	S2	OFF	→	ON	→	OFF	→	ON	→
	S3	OFF		OFF		OFF		OFF	
	S4	OFF	→	ON	→	OFF	→	ON	→
	S5	OFF		OFF		OFF		OFF	
	S6	OFF	→	ON	→	OFF	→	ON	→
	S7	ON	→	OFF	→	ON	→	OFF	→
	S8	OFF	→	ON	→	OFF	→	ON	→
	S9	ON	→	OFF	→	ON	→	OFF	→

TABLE 5.7: Comparison between number of MOSFET switchings

	Conventional SCVR	MMVR without PIT	MMVR with PIT
First Operation Region	16	14	14
Second Operation Region	28	26	18
Third Operation Region	28	14	14

5.4 Controller Structure

Since the MMVR has its unique operation principle that has not been used before, generating the controlling signals of switches is not a straight forward process. A novel optimized controller structure for generating the complex switch driving waveforms has been proposed. Some complexity is added to the controller structure compared to that of conventional voltage regulators as a price for the enhanced performance. However, since the controller circuit is fully digital-based, this is not considered as an issue in modern CMOS technologies. One can look at this voltage regulator as if the complexity is shifted from analog part of the VR towards digital part which is a preferable trend in modern CMOS technologies.

In this section, the controller structure of the 4-level 4-state VR is discussed in detail as it is considered the brain of the regulator. As stated previously, in the 4-level 4-state VR, a one complete switching cycle is divided into four time slots; each time slot has its own controllable duration relative to the main switching cycle. The switching cycle starts at the positive edge of the main system clock and ends at the next positive edge. In each time slot, each switch in the circuit may be turned on or off depending on the desired SCC configuration in that time slot. Figure 5.8 shows an example on switch driving waveforms in the second operation region with phase interleaving and with a main duty cycle of half. The controlling of each time slot duration is done based on Pulse Width Modulation

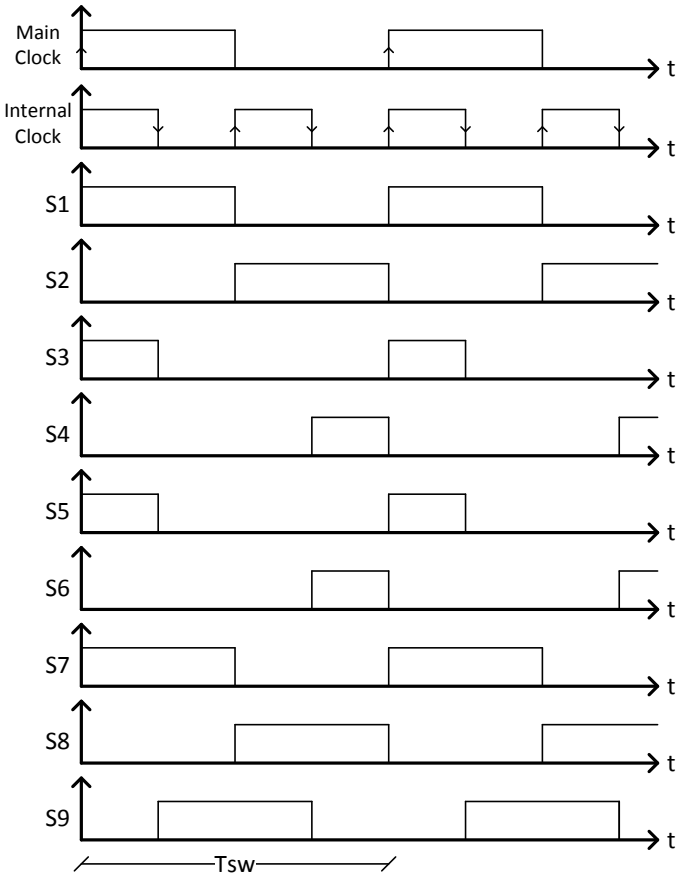


FIGURE 5.8: Switch driving waveforms in second operation region generated from main system clock

(PWM) technique which is the main controlling scheme of the proposed MMVR. The PWM is a well-known technique used widely in voltage regulators as well as other applications and has been described and analyzed in many literature work [37–39].

The full structure of the proposed digital controller is shown in figure 5.9. It consists of a normal compensator which is an essential block in any voltage regulator. The compensator takes into consideration the dynamic response of the voltage regulator and compensates for it to ensure the VR stability and enhance its transient response in react to fast changes in load current, input voltage or reference voltage. The compensator takes the reference voltage and the current

output voltage as an input and generates a correction signal. The correction signal then goes as an input to the waveform generation block that determines the required operation region and duty cycle values and generates the required driving waveforms for the switches.

The waveform generation block consists of several sub-blocks as shown in figure 5.9. First, the correction signal coming from the compensator goes as an input to a block that determines, firstly, desired operation region, secondly, main duty cycle value inside that operation region, and thirdly, internal duty cycle values of the two voltage levels of that operation region. After that, the calculated main and internal duty cycle values go as an input to a Digital Pulse Width Modulator (DPWM) that is responsible for generating an internal clock from the system clock. The system main clock comes from a clock generator with a period equal to that of one switching cycle.

The DPWM has its well-known structure developped in literature work [37, 38]. However, in the MMVR, some modifications have to be added to the DPWM structure to be able to generate a signal with four controllable-duration regions (rather than one) from the main system clock. There are two main techniques to build a DPWM, the counter-based technique and the delay technique. Since integrated voltage regulators in general are working at a frequency in the range of hundreds of MHz, the counter-based technique is not feasible since it will require a clock with a very high frequency. Therefore, the delay line technique is used. The proposed DPWM structure to perform this task consists of only one delay line followed by three multiplexers. The selection bits of these three multiplexers are calculated from the main and the internal duty cycle values. The outputs of the three multiplexers are delayed versions of the main system clock by an amount equal to (T1), (T1 + T2) and (T1 + T2 + T3) where T1, T2 and T3 are the durations of the first, second and third time slot respectively.

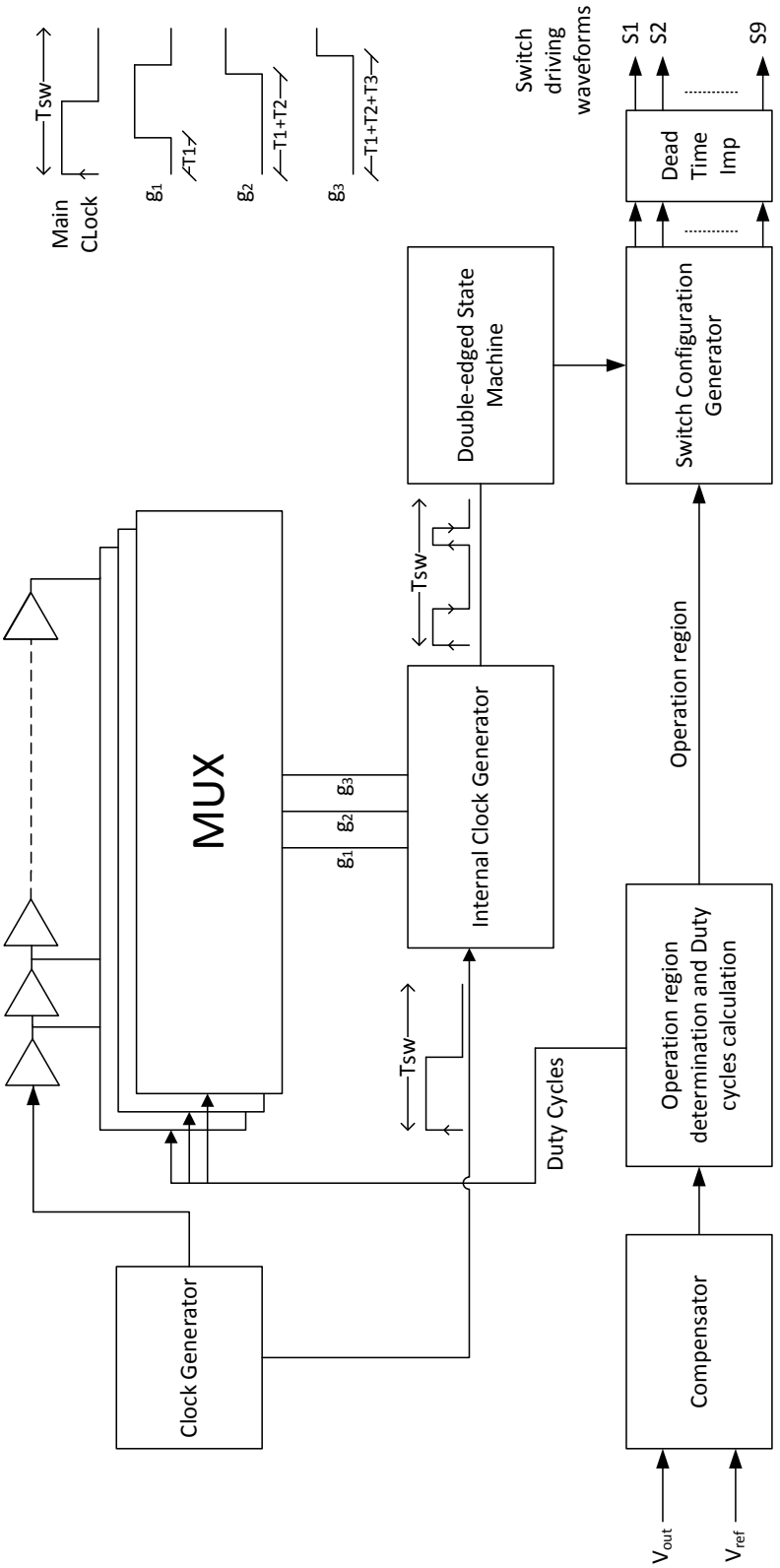


FIGURE 5.9: Controller Structure of 4-level 4-state Voltage Regulator

The output of the three multiplexers besides the main system clock goes as an input to the internal clock generation block. This block uses a combination of set/reset flipflops (SRFFs) besides some combinational circuits to generate an internal clock with four edges (-ve and +ve edges). The duration between each two edges represents the duration of one of the four time slots of the switching cycle.

After that, the generated internal clock works as a double-edged clock for a state machine block which goes to the next state at each +ve or -ve edge of the internal clock. The state machine consists of four states representing the four time slots of one switching cycle. In each of these states, there is a certain configuration for the switches depending on the operation region the VR is working at. The current and the desired operation region go as an input to the switch configuration block which stores the switches configuration in each operation region. Depending on the current state and the operation region desired, the switch configuration gives as an output the switches configuration in this state giving a high signal if the switch is on and low signal if the switch is off in that state. The switch configuration block can be implemented in two ways. The first way is to use a combinational circuit that takes the state number and the operation region as an input and gives as output the configuration of each switch. The second way is to use an SRAM to store the switches configuration in different operation regions. The SRAM has nine outputs representing the nine switches configuration and gives its output at the start of each state.

After the nine driving waveforms of switches are generated from the switch configuration block, they pass through a dead time implementation block to prevent overlapping between signals so that no short circuit current happens when some switches become simultaneously on at wrong time. After that, the nine driving waveforms are ready to drive the switches of the SCC. The dead time can be fixed or varying. A varying dead time may result in a higher performance by accounting for process variations by would require a more complicated control circuit. The

working procedure of the controller is as follows: at the start of each main clock edge, the compensator senses if there is a difference between the reference and the current output voltage and generates a correction signal. If the correction signal is small then just an adjustment in the main duty cycle value may be enough while staying in the same operation region. The determination block gives a new main duty cycle command to the DPWM which adjusts the duration of the internal clock segments to give the required output voltage value. On the other hand, if the correction signal is large enough which means a big change in output voltage is required, the determination block chooses the new appropriate operation region along with the main and internal duty cycle values required to give desired output voltage and gives these commands to the DPWM and Generator block. Therefore, a coarse and fine tuning of output voltage are achieved through the controller.

5.5 Circuit Implementation

The 4-level 4-state VR circuit has been built on standard CMOS technology to verify its performance and compare it with other conventional two types of voltage regulators. First, some guidelines on sizing the different components of the voltage regulator are provided. After that, two designs for the 4-level 4-state voltage regulator implemented on two different technologies are provided where, in each design, the inductor is realized using a different technique.

5.5.1 Component Sizing

Flying capacitor size has a direct impact on the power density of the voltage regulator. In most voltage regulators, the capacitors are the dominant consumer of the voltage regulator area and in most cases their sizes are limited by the area budget given to the voltage regulator. Beside the power density, the flying capacitor affects the performance of the voltage regulator as well. Figure 5.10 shows

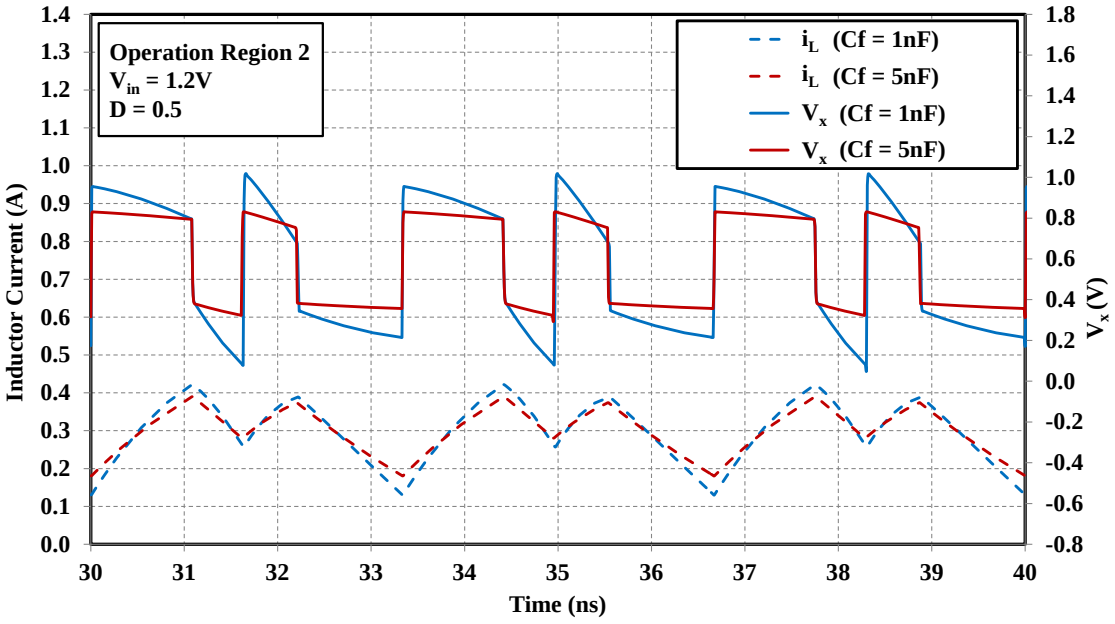


FIGURE 5.10: Simulation of SCC output voltage (V_x) and corresponding inductor current (i_L) for two different flying capacitor sizes

the SCC output waveform (V_x) and the corresponding inductor current (i_L) for two different flying capacitor sizes. The variations in the output voltage level from SCC at each state, as appears in figure 5.10, is due to the ΔV drop that happens on flying capacitors during charging and discharging process. As mentioned previously, the ΔV on flying capacitors results in higher inductor current ripples which in turn increases conduction losses. This ΔV on flying capacitors can be decreased by either increasing the flying capacitor size, as shown in figure 5.10, or increasing the switching frequency. On the other hand, increasing the flying capacitor size means higher bottom plate parasitic capacitance that causes more switching losses. Therefore, a flying capacitor size that achieves a good balance between these different losses within the area budget limit would be the optimum choice to get the best performance.

The inductor size is the main concern in integrated voltage regulators. As illustrated previously, the MMVR results in a reduced inductor size while maintaining same performance (i.e. same peak-to-peak current ripples). In general,

the trade-offs in inductor size come from its equivalent series resistance. For a certain technology with a certain quality factor for the inductor, the larger the inductor size, the higher its equivalent series resistance (R_{ind}). On the other hand, a smaller inductor size means higher inductor ripples as depicted in equation 4.2 and hence higher RMS value for the inductor current. The conduction losses in the inductor ($P_{cond,ind}$) is given by:

$$P_{cond,ind} = I_{RMS}^2 R_{ind} \tag{5.12}$$

As inductor size increases, R_{ind} increases but I_{RMS} decreases. Hence, according to the equation, there is an optimum inductor size that results in lowest $P_{cond,ind}$. In another aspect, the inductor size has a direct impact on flying capacitor stability as shown in figure 5.2. Smaller inductor sizes ensures more stability for the average voltage on flying capacitors and hence a reliable and constant output voltage from SCC. The inductor size affects the output voltage ripples in an indirect way. This is because the inductor current ripples go into the output capacitor and are translated into output voltage ripples. Hence, the peak-to-peak output voltage ripples have a direct relation with the peak-to-peak inductor current ripples.

The switches' sizes play the conventional known role in balancing between conduction and switching losses. However, this trade-off is somewhat relaxed here because the MMVR results in a reduced number of switching MOSFETs in one switching cycle opening the room for an enhanced performance in general. The optimum size for each switch from the nine switches of the 4-level 4-state VR is not necessarily the same because the current flowing in each switch is not the same and their on-time as a percentage from one switching cycle is not the same as well. A procedure like the one used in [30] is used in this design to optimally size the switches.

The size of the output capacitor has a direct impact on output voltage ripples. The higher the output capacitor size, the lower the output voltage ripples. In another aspect, the output capacitor has a minor effect on VR efficiency because of its parasitic equivalent series resistance. This parasitic resistance causes conduction losses by the RMS value of the current flowing inside the output capacitor. These effects should be taken into consideration while sizing the output capacitor.

5.5.2 Design One: Using On-chip Spiral Inductors

In this design, the 4-level 4-state VR circuit was implemented on TSMC 65nm standard CMOS technology using on-chip spiral inductors. Table 5.8 shows the voltage regulator specifications. The inductor was realized using 1nH on-chip spiral inductor with a quality factor of (4.7). A boost driver like the one in [30] is used to drive MOSFETs that are transferring high voltage values (i.e. near V_{in} level) to achieve higher overdrive voltage and thus lower on-resistance. The switches configurations are generated using an analog verilog (verilogA) model.

TABLE 5.8: Voltage regulator specifications for design one

Parameter	Value
Technology	TSMC 65nm
Input voltage (V_{in})	1.2V
Output Voltage (V_o)	0.2V - 1.1V
Maximum output current	300mA
Maximum output power	0.33W
Inductor (L)	1nH (On-chip spiral inductor)
Flying Capacitors (C_f)	2×1.5nF (MIM Caps)
Output Capacitor (C_o)	10nF (MOS Caps)
Switching frequency (F_{sw})	200MHz
Maximum efficiency (η_{max})	90%

Figure 5.11 shows a comparison between the efficiency of 4-level 4-state VR and triple-ratio switched capacitor VR with an inductor to eliminate charge sharing

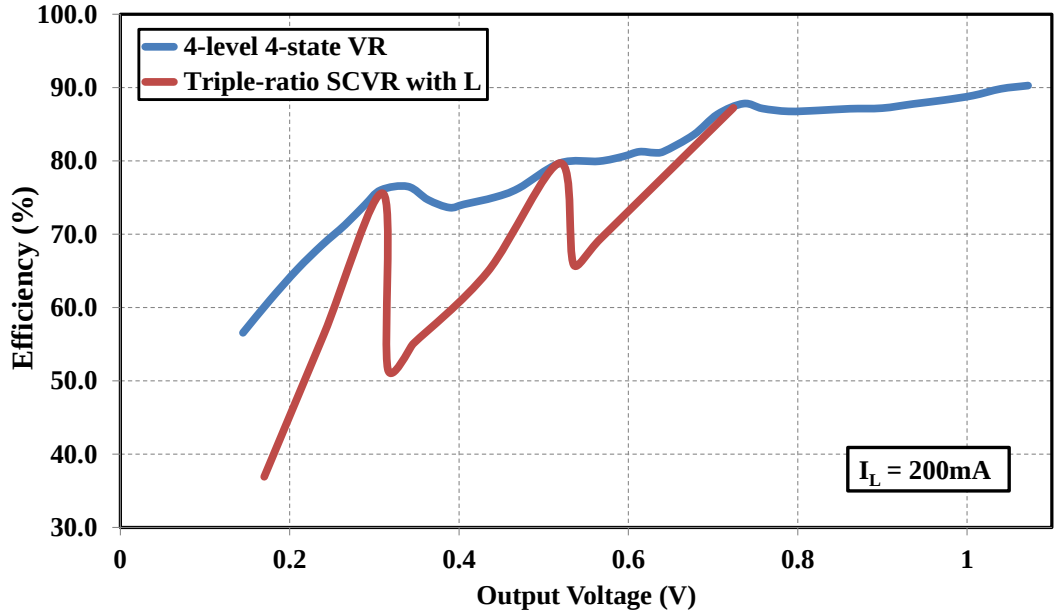


FIGURE 5.11: Simulated efficiency comparison between 4-level 4-state VR and switched-capacitor VR with a series inductor

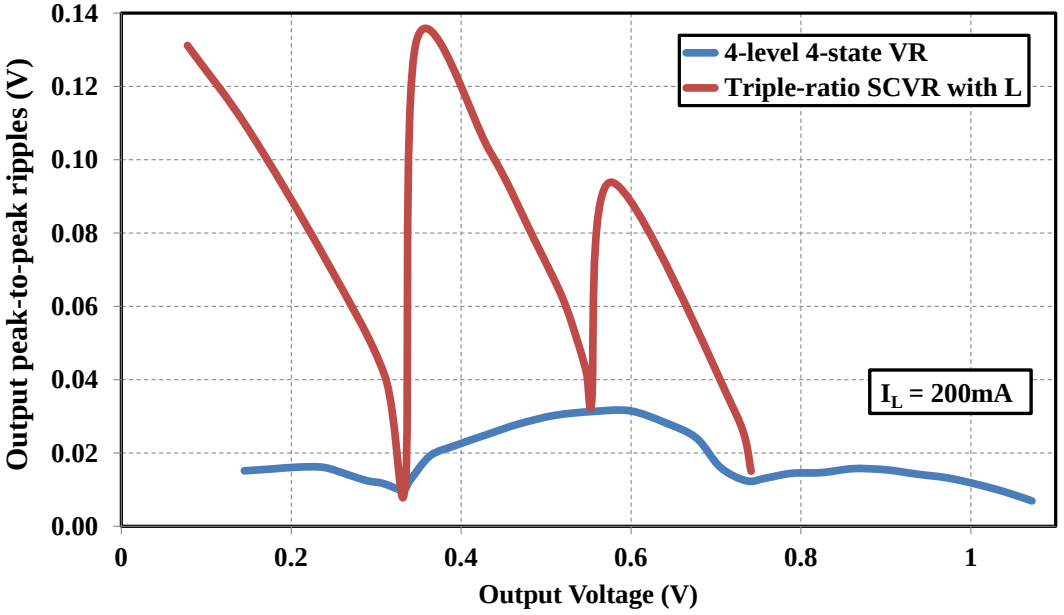


FIGURE 5.12: Simulated output voltage ripples comparison between 4-level 4-state VR and switched-capacitor VR with a series inductor)

losses [33]. The strong regulation capability of MMVR using PWM control scheme can be noticed. The efficiency of the switched capacitor circuit starts to degrade once deviating from normal output voltages of three conversion ratios as can be seen in figure 5.11. This enhanced regulation capability can be noticed as well when comparing between peak-to-peak output voltage ripples of both types as depicted in figure 5.12. It can be noted that both regulators have the same efficiency and output voltage ripples at the three normal output voltages because at the edges of each operation region, the 4-level 4-state VR is operating like a switched-capacitor VR with an inductor.

5.5.3 Design Two: Using Wire-bond Inductors

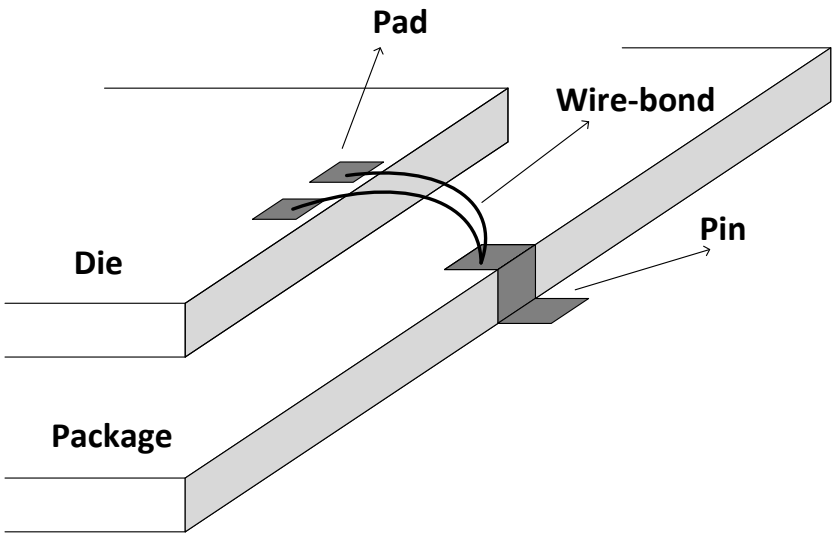


FIGURE 5.13: Inductor realization using parasitic inductance of package wire bond

Another implementation of 4-level 4-state voltage regulator is done on Global-Foundries 65nm standard CMOS technology. In this implementation, the inductor is realized using package bond-wire parasitic inductance as shown in figure 5.13 which is the same technique used in [14, 40]. In this technique, the inductor is realized by going off chip to a pin through a wire-bond then returning back from the

same pin to another pad on the die through another wire-bond. This technique has an overhead of utilizing two pins but it offers an inductor with good characteristics (i.e. good quality factor). However, there is uncertainty in the inductance value due to process variations when building the wire-bonds. The circuit is designed to accommodate for these variations in inductance value which can be in the range of 2nH to 10nH. Table 5.9 shows the voltage regulator specification.

TABLE 5.9: Voltage regulator specifications for design two

Parameter	Value
Technology	GF 65nm
Input voltage (V_{in})	1.2V
Output Voltage (V_o)	0.4V - 1.1V
Maximum output current	200mA
Maximum output power	0.22W
Inductor (L)	3-10nH (wire-bond package inductance)
Flying Capacitors (C_f)	2×2.25nF (MIM Caps)
Output Capacitor (C_o)	10nF (MOS Caps)
Switching frequency (F_{sw})	100MHz
Maximum efficiency (η_{max})	93%

Transmission gates are used as a switch at the nodes of varying voltage depending on operation region. The transmission gate can then pass both high (near V_{in}) and low voltage (near ground) when it is on. At high voltage, pMOS is mainly working on while at low voltage, nMOS is working mainly. At intermediate voltages, both nMOS and pMOS are on with their on-resistance connected in parallel resulting in lower on-resistance. Thus, an almost constant on-resistance over the whole voltage range is achieved. The advantage of using transmission gates as switches is that their driver circuitry are simpler than other drive schemes.

A digital controller with a structure like the one showed in figure 5.9 is implemented on GF 65nm with an ASIC flow using ARM standard cells. A precise design of the delay line in the DPWM is required to allow for accurate control

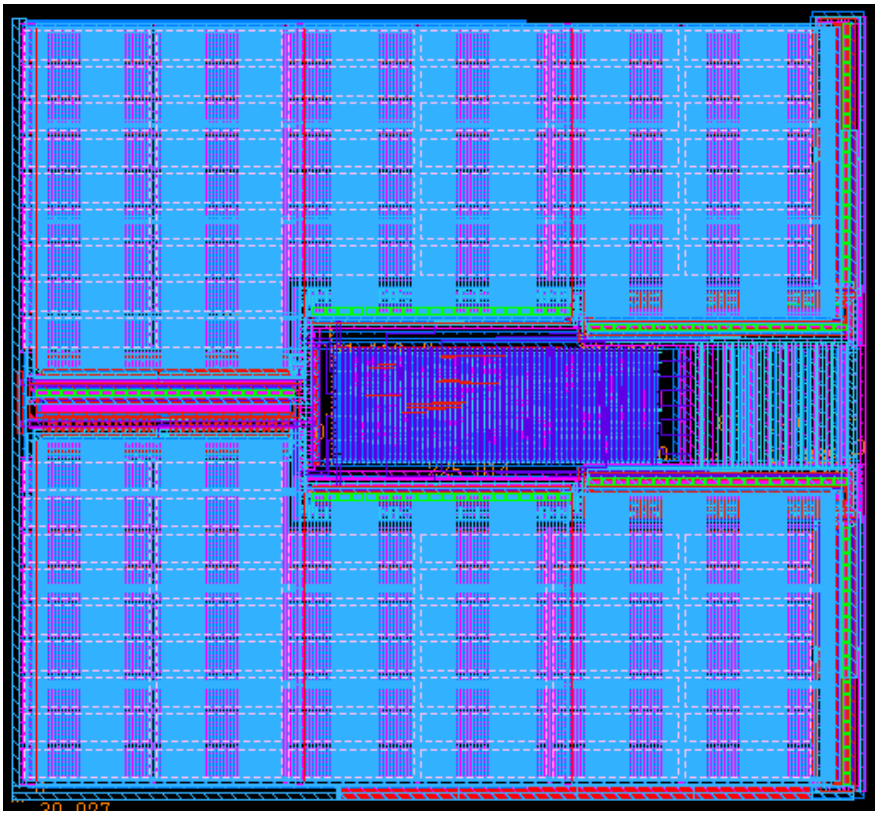


FIGURE 5.14: Full layout of the voltage regulator circuit on GF 65nm

of duty cycle value at a switching frequency of 100MHz. The output capacitor is realized using MOS capacitors and is placed under the flying capacitors which are realized using MIM capacitors so that the area is utilized efficiently. Figure 5.14 shows a snapshot of the full layout of the VR circuit ready to be fabricated on GF 65nm. The voltage regulator circuit consumes a total silicon area of $2.5mm^2$. All results mentioned in this section for 4-level 4-state VR are from post-layout simulations.

Figure 5.15 shows a comparison between the efficiency of the 4-level 4-state VR after post layout simulation and a triple-ratio switched-capacitor VR. As observed in design one, the efficiency of switched capacitor voltage regulator starts to degrade quickly when deviating from normal operation points. This is mainly because of their lossy regulation scheme where the output voltage is regulated using switching frequency. This is not the case in 4-level 4-state VR where the output is

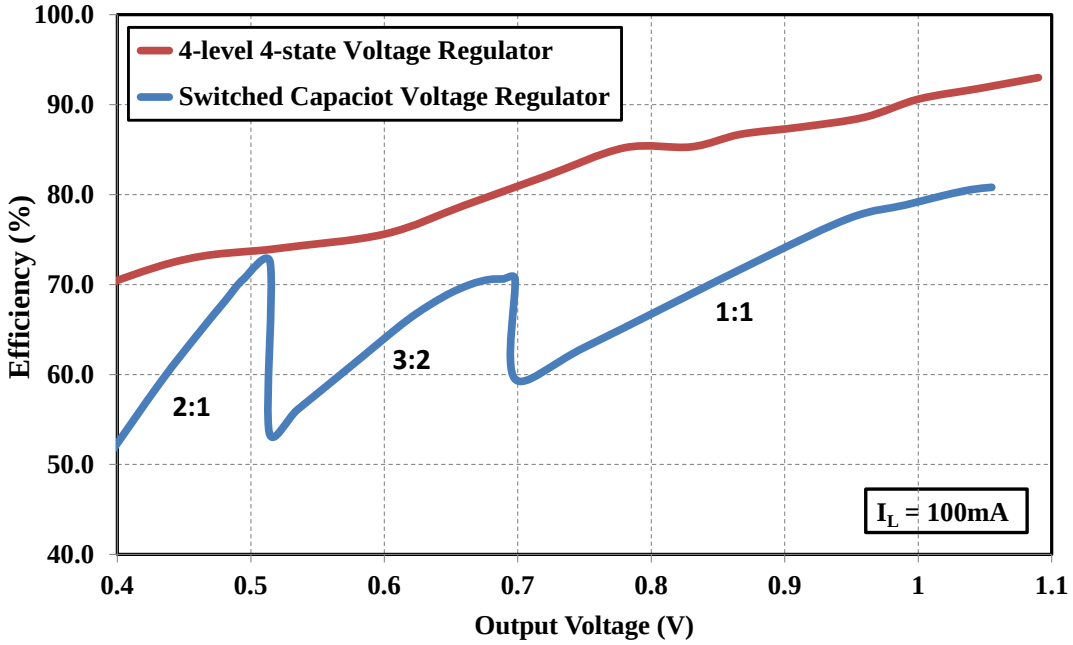


FIGURE 5.15: Simulated efficiency comparison between 4-level 4-state VR and switched-capacitor VR

regulated using PWM technique which is an efficient regulation scheme. Moreover, the 4-level 4-state VR has an overall higher efficiency than switched-capacitor VR. This is mainly because the charge sharing losses that exist in switched-capacitor VR are almost eliminated in 4-level 4-state VR due to the existence of the inductor that restores these losses.

Figure 5.16 shows a comparison between the efficiency of the 4-level 4-state VR and a conventional buck converter using the same inductor size and operating at same frequency. It can be noticed that the 4-level 4-state VR has a higher efficiency in general which is almost 10% higher than conventional buck converter one. This is mainly because the 4-level 4-state VR exibits lower inductor ripples compared to conventional buck converter as explained previously. Hence, the conduction loss of the 4-level 4-state VR is lower than that of conventional buck converter. Table 5.10 shows a comparison with some state-of-the-art integrated voltage regulators. The proposed VR offers better performance compared to other literature work.

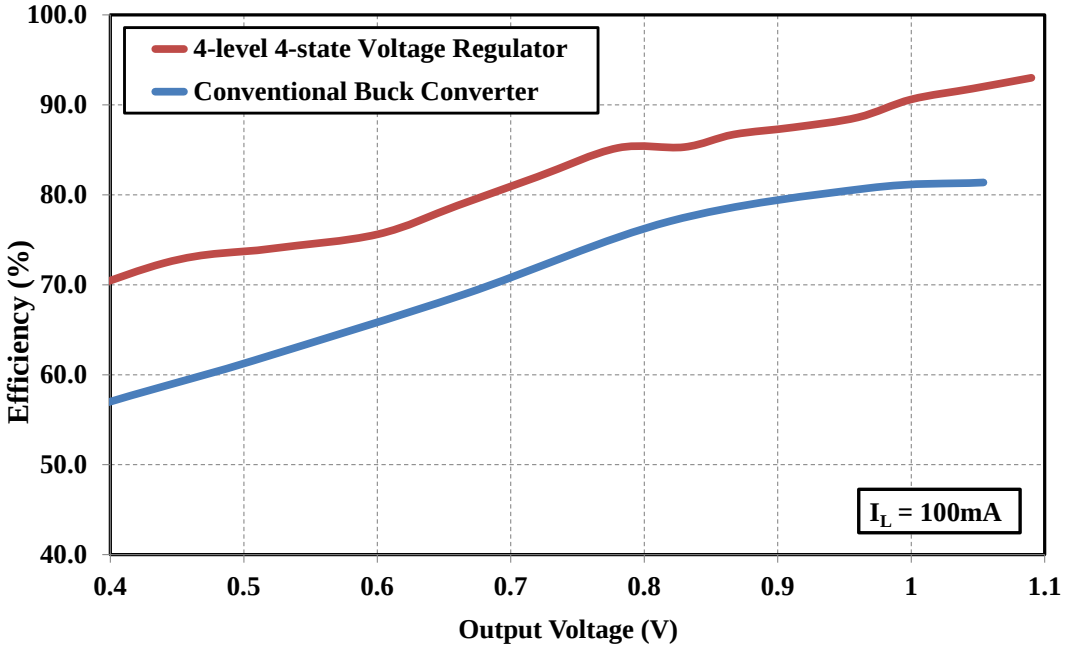


FIGURE 5.16: Simulated efficiency comparison between 4-level 4-state VR and conventional buck converter

TABLE 5.10: Performance comparison with previous work

	[15]	[41]	[22]	[42]	[43]	[14]	This Work
Year	2008	2010	2011	2011	2012	2013	2014
Technology	130 nm	45 nm	130 nm	130 nm	130 nm	130 nm	65 nm
Topology	Buck	SC	3Level	Buck	Buck	Buck	Hybrid
Switching Frequency	170 MHz	30 MHz	200 MHz	250 MHz	50 MHz	100 MHz	100 MHz
Inductor/ Capacitor	2 nH x 2 (Spiral)	0.53 nF (MOS)	1 nH x 4 (Spiral)	4.5 nH (Spiral)	19.9 nH (Wire-Bond)	3 - 10 nH (Wire-Bond)	3 - 10 nH (Wire-Bond)
Output Capacitor	5.2 nF	0.7 nF	10 nF	7 nF	3.4 nF	9.8 nF	10 nF
Input Voltage	1.2 V	1.8 V	2.4 V	1.2 V	3.3 V	1.2 V	1.2 V
Output Voltage	0.9 V	0.8 - 1 V	0.4 - 1.4 V	0.9 V	2 V	0.9 V	0.4 - 1.1 V
Max Load Current	350 mA	8 mA	600 mA	172 mA	300 mA	370 mA	200 mA
Peak Efficiency	77.9%	84%	77%	80 %	76.8%	84.7%	93%
Chip Area	$1.5mm^2$	$0.16mm^2$	$5mm^2$	$3.92mm^2$	$10.1mm^2$	$2.25mm^2$	$2.5mm^2$

5.6 Summary and Conclusion

In this chapter, a 4-level 4-state Voltage Regulator has been proposed. The VR circuit is built based on the MMVR general structure and operation techniques discussed in chapters 3 and 4. The operation of the VR as well as analysis for its functionality and performance have been provided along with some illustrating examples and tables. A controller structure to operate the 4-level 4-state Voltage Regulator has been proposed. After that, a full implementation of the circuit on TSMC 65nm has been done to verify the VR performance. The VR performance was compared to other literature work showing that the MMVR offers a significant improvement in performance compared to other literature VRs. This proves that the proposed MMVR set may be considered as an optimum solution to challenges of integrated voltage regulators.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

In this work, a new set of voltage regulators has been proposed. They are capable of providing step up, step down or step up/down voltage conversion. The two main types of voltage regulators have been evaluated with a focus on the main limiting factors of each type. These limitations introduce challenges and cause performance degradation when integrating voltage regulators on chip. Some trials to overcome the limitations of each type have been reviewed. It was concluded based on these trials that both main types of voltage regulators are evolving to the same point which is a hybrid structure between the two types which seems to be the optimum point.

The proposed multilevel multistate voltage regulator covers this gap between inductor-based and capacitor-based voltage regulators. The general structure of the proposed voltage regulator and its working principle are illustrated. A comparative analysis with both main types shows that MMVR is offering solutions to the limiting factors of each type. This is achieved by taking the advantages of both types while avoiding or minimizing their drawbacks. Therefore, the proposed

voltage regulator offers an optimum solution to challenges facing modern voltage regulators.

The phase interleaving technique has been proposed which is a novel controlling scheme that can be used to operate the MMVR. This technique can boost the performance of the MMVR by enhancing the effective switching frequency of its individual components. Some metrics or factors to compare between the performance of MMVR with and without phase interleaving technique have been introduced.

A 4-level 4-state voltage regulator has been introduced as an implementation of MMVR. All the aforementioned methods and techniques are applied and validated in the 4-level 4-state VR. Two different implementations for 4-level 4-state VR have been done using two different techniques to realize the inductor. The results are compared with conventional two types of voltage regulator and with recent literature work in VRs showing that the 4-level 4-state voltage regulator offers significant performace improvements.

Many VR circuits based on MMVR general structure and concepts can be developed. Figure 6.1 shows another circuit implementation for MMVR which is a 5-level 8-state VR as a proof of generality and scalability of proposed voltage regulator structure and controlling schemes. In the 5-level 8-state voltage regulator, the SCC is providing five voltage levels and the switching cycle is divided into 8 states. Along with wide variety of available implementation of MMVRs, some implementations may be the most suitable for certain application under a given technology. To conclude, the MMVR is a proposed general structure for voltage regulators offering potential solutions to challenges in modern VRs.

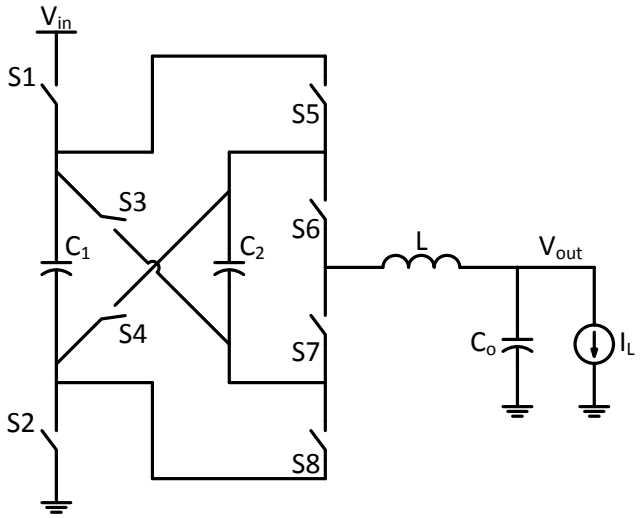


FIGURE 6.1: Another implementation of MMVR: 5-level 8-state Voltage Regulator

6.2 Future Work

Future work may include building more topologies and testing their performance. What has been provided here is a general framework for a new set of voltage regulators. Many implementations based on these concepts and techniques can be done as a future work along with more analysis to get a deeper insight on the MMVR.

More study on the flying capacitor stability is another way to go through. The factors affecting the voltage on flying capacitors need more investigation as well as the effect of imbalanced flying capacitors on the MMVR performance. This is to ensure more stable and reliable operation of multilevel multistate voltage regulators.

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