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New mathematical formulation for designing a fully differential self-biased folded cascode amplifier

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NEW MATHEMATICAL FORMULATION FOR DESIGNING A FULLY DIFFERENTIAL SELF-BIASED FOLDED CASCODE AMPLIFIER

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ABSTRACT

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New Mathematical Formulation For Designing A Fully Differential Self-Biased Folded Cascode Amplifier

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One of the most important building blocks in analog circuit design is the operational amplifiers. This is because of their versatility and wide spread usage in many applications such as communications transmitters and receivers, analog to digital converters, or any other application that requires a small signal to be amplified. The basic amplifier topologies are introduced. Then, some operational amplifiers topologies are introduced with some techniques to self bias these amplifiers. The folded cascode fully differential Op-Amp with self bias is presented. This is one of the newest amplifier topologies which provide stable self-biased amplifiers. A new mathematical model for fully differential folded cascode amplifiers is presented and generalized to include the family of fully differential complementary amplifiers. This formulation focuses on deriving detailed design equations for the amplifier gain and frequency response. The equations are verified through time domain and frequency domain simulations of different fabrication processes to ensure the validity of the model across a wide range of processes. The model was verified against TMSC 180nm, 250nm, and 350nm fabrication processes. The new model agrees well with simulations; with 1% error for the amplifier gain and <7% error for amplifier bandwidth. The relatively high error value for the bandwidth is because the model considers the worst case scenario and overestimates the output capacitance. Finally, the algorithm of getting this formulation is extended to include special and commonly used cases. This formulation proved to be very useful in designing stable, self-biased, fully differential folded cascode amplifiers.

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A. Introduction to Amplifiers

One of the most important topics in electronic circuit design is analog circuit design which differs from digital circuit design in the nature of signals to deal with. Its importance comes from the fact that the entire physical world with its phenomena is represented on a continuous scale such as temperature, speed, distance…etc. This makes it more natural to use analog circuits when dealing with such quantities. On the other hand, digital circuit design only deals with zeros '0' and ones '1' and it uses a combination of them to represent any physical quantity which is only possible when the appropriate conversion devices which are called analog to digital converters are used. However, this ease of representation comes with a price. Usually, analog circuit design is more complex and has to take care of certain circuit requirements and include some components that do not exist in the digital domain.

One of the most important building blocks in analog circuit design is the signal amplifier. Amplification is one of the most crucial functions in analog circuit design. For example, the need for amplification emerges when a load has to be driven by a small input signal, or when the noise from the next stages in the design has to be cancelled …etc. Before going into much detail about amplifiers, amplifier characterization parameters have to be described. The most important property of an amplifier is its open-loop gain

which is simply the ratio between the output to the input of the amplifier. The open loop gain is usually required to be as high as possible such that when connected in a closed loop configuration, the overall circuit gain would depend only on the feedback circuit. Another important property is the amplifier frequency response which determines the maximum signal frequency that can be used without too much degradation in the circuit performance. This is determined by the sizes of the devices used and their parasitic capacitances which mainly depend on the fabrication process. Another important characteristic is the stability of the amplifier which determines the maximum amplitude and frequency that the amplifier can handle and still produce the proper output. In addition, there are other characteristics such as the area of the amplifier, its power consumption, output and input voltage swings…etc. which differ from one amplifier to another [1].

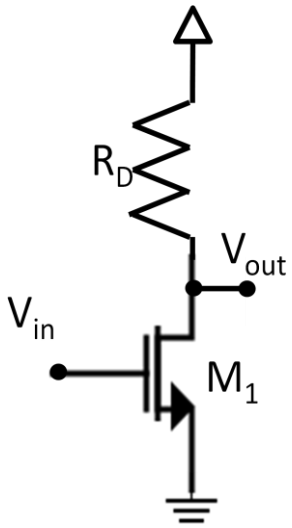

Figure 1: Common Source Amplifier with Resistive Load [1]

Amplifiers exist in many topologies and implementations. Each one has its own characteristics and applications. For example, Figure 1 shows the

simplest voltage amplifier topology. It consists of one device M1 which converts the input voltage into current that passes through the load R1 giving a gain that can be described by the following equation:

$$Gain = -g_m \times R_D \qquad (1)$$

Where g_m is the trans-conductance of the transistor M1 and R_D is the value of the load resistance. Different variants can be derived from the common source amplifier by simply changing the terminals for the input and the output. This provides us with two more topologies: the common gate amplifier and the common drain amplifier as shown in Figure 2. In many cases, the load resistance in the amplifier is replaced by another transistor. This has the advantage of decreasing the size of the circuit because the area needed to implement a resistor on an electronic chip is much larger than that needed to implement a transistor. However, this makes the design problem more difficult and produces more parasitic elements due to this added device.

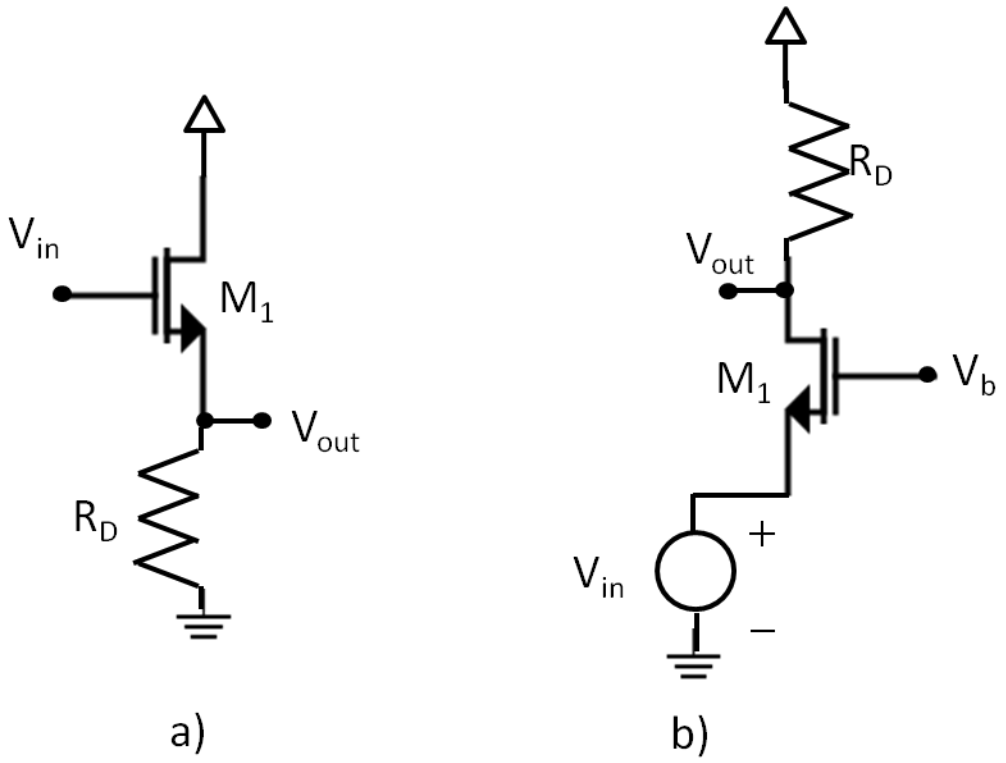

Figure 2: Different Amplifier Topologies [1]

a) Common Drain (source follower) configuration

b) Common Gate Configuration

Many applications require much more gain than that provided by these simple amplifiers. Also, in many cases, the signal to be amplified is provided in differential mode i.e. difference between two voltages. Hence, amplifiers which can accept two inputs and produce up to two outputs had to be implemented. This type of amplifier is called a differential amplifier. It can be constructed from any of the aforementioned configurations. Figure 3 shows the basic differential amplifier [1].

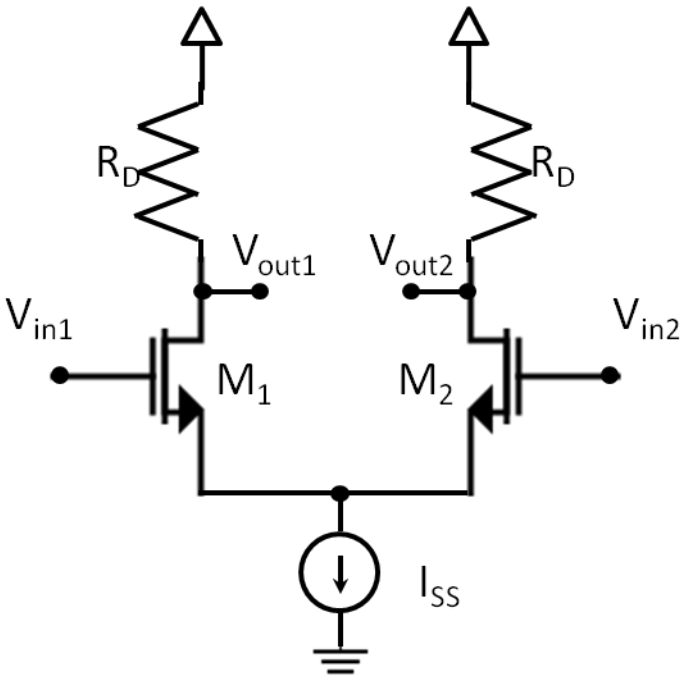

Figure 3: Basic Differential Amplifier [1]

As discussed in the case of single input amplifier, differential amplifiers can be implemented using different topologies. In case of higher gain requirements, amplifiers are usually cascaded to achieve higher gain values. However, this makes the design problem very difficult and introduces the concept of frequency compensation which is needed to stabilize the amplifier after adding the second stage. This report will focus on the gain aspect of differential amplifiers as they are widely used and can provide the gain requirements for many applications [1].

B. Literature Review

From the previous introduction, it can be noted that amplifiers have many topologies each with its own characteristics that make it fit certain types of applications. Also, it is noted that each application requires a specific set of requirements that the amplifier needs to meet such as the gain, frequency response, speed…etc. This makes the design process of an amplifier a tedious task. In addition to that, the properties of analog circuits do not scale easily between fabrication technologies and between different applications. Hence, many researchers are interested in finding an efficient topology that fits most of the applications and are interested in finding a design process that enables engineers to meet the application requirements in a timely manner with high accuracy. Multiple amplifier topologies have been designed over time to meet different process requirements and to overcome fabrication process scaling challenges [2-5].

In the literature, amplifiers are usually referred to by the name operational amplifiers or Op-Amps in short. These naming standards shall be used interchangeably for the rest of the work. According to Aminzadeh et al. [6], Op-Amps are used extensively in analog and mixed-signal circuits. For example, voltage regulators, filters, and data converters use Op-Amps to buffer, filter, amplify signals…etc. Also, the authors pointed out that single stage Op-Amps are superior to multi stage Op-Amps in terms of speed and frequency response. That is why this work will only focus on single stage differential amplifiers. Furthermore, Op-Amps play a crucial role in many other applications such as communications transmitters and receivers, analog

to digital converters [7-10], Micro Electro-Mechanical Systems (MEMS) sensor oscillators, etc [11-15].

One of the commonly used Op-Amp topologies is the folded cascode topology [16-18]. According to [19], simple folded cascode Op-Amps display a single pole frequency response that is characterized by a large unity gain frequency but with relatively low gain. This was improved through gain boosting techniques. Figure 4 shows an example of the gain boosting techniques. This made the folded cascode amplifier meet the high gain requirement needed for fast settling.

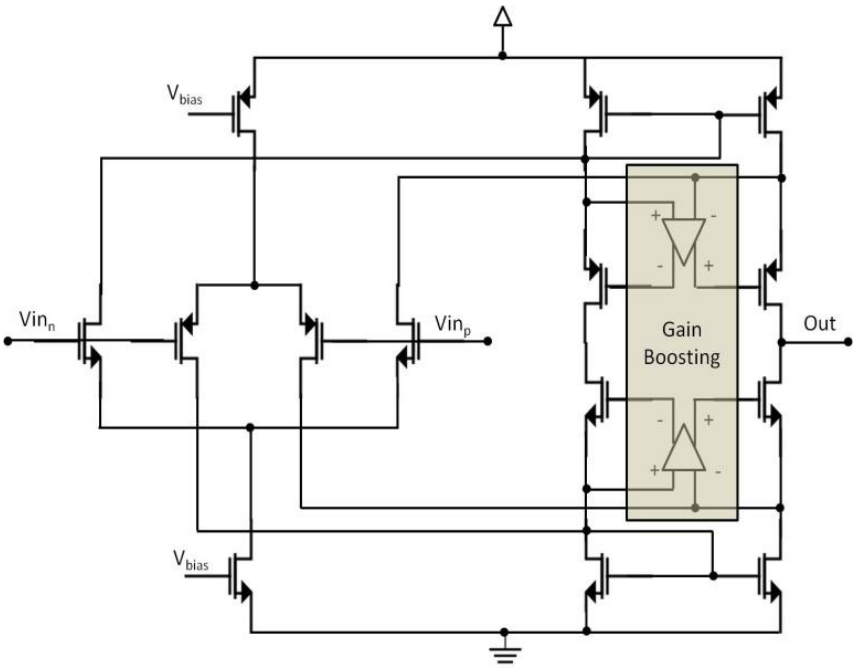

Figure 4: Folded Cascode Amplifier with External Biasing [19]

However, this technique needed too many external supply voltages to provide the correct bias point required for the Op-Amp to function properly. Using many external supply voltages caused other problems such as higher

power consumption, higher susceptibility to noise and cross-talk in the bias lines, and higher sensitivity to fabrication process variations. Consequently, techniques of self biasing folded cascode Op-Amp were investigated to eliminate the need for external bias sources [4] [20-21]. Figure 5 demonstrates an example of the commonly used self biasing techniques. This technique simply used an internal voltage node to bias the current sources used in the Op-Amp. This eliminated the sensitivity to process variations because the voltage on this internal point changes in accordance to these variations. Also, the extra power sources were eliminated and with them the noise and cross talk were eliminated as well. However, this technique reduced the slew rate for the amplifier due to reduced gain. This was compensated for using properly sized transistors that use a little bit more area in order to maintain the same performance given by the unbiased folded cascode Op-Amp [19].

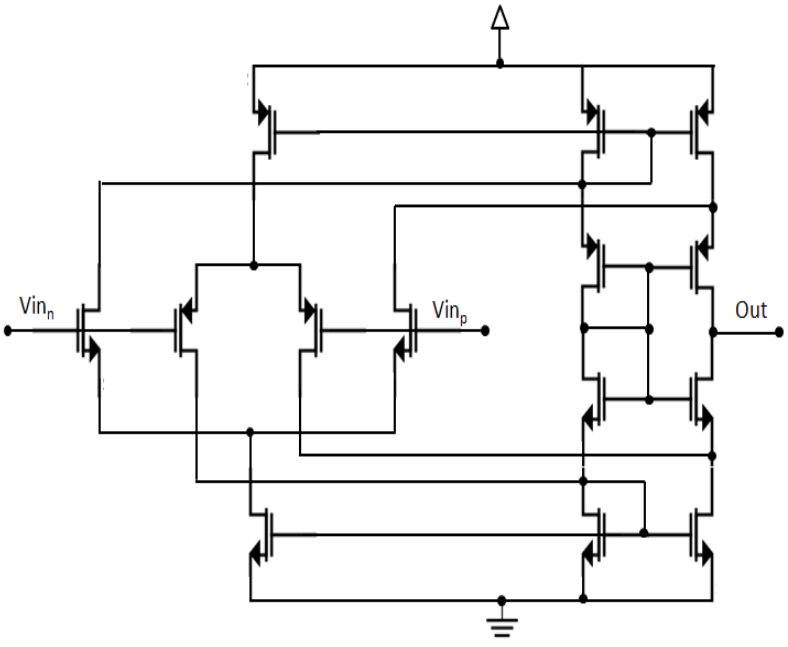

Figure 5: Self Biased Folded Cascode Op-Amp [19]

The biasing problem captured the attention of many researchers as the correct biasing point ensures the correct functionality of the entire circuit [22-23]. Furthermore, this biasing point can be affected by many parameters such as the fabrication process variations. Consequently, self biasing techniques became a very viable solution for these variation problems. Bazes [24] designed two different amplifiers to solve the biasing problem. One of these amplifiers is the Very wide Common mode Differential Amplifier (VCDA). This amplifier works best when the input signal has a very wide common mode range. This is because the proposed amplifier is complementary which means that every device in the amplifier is matched with its dual device. This guarantees that when the input signal exceeds the operation range for one device, its dual will be functioning properly. This amplifier was derived from two separate, but complimentary, folded cascode amplifiers through replacing their respective loads by the other amplifier. Then, to make the amplifier self biased, one of the output nodes was used to bias all the current sources in the amplifier. This design process is illustrated in figure 6. This technique provided a very stable method to bias the amplifier, but it dictated that one of the output nodes was used to bias the current sources [24].

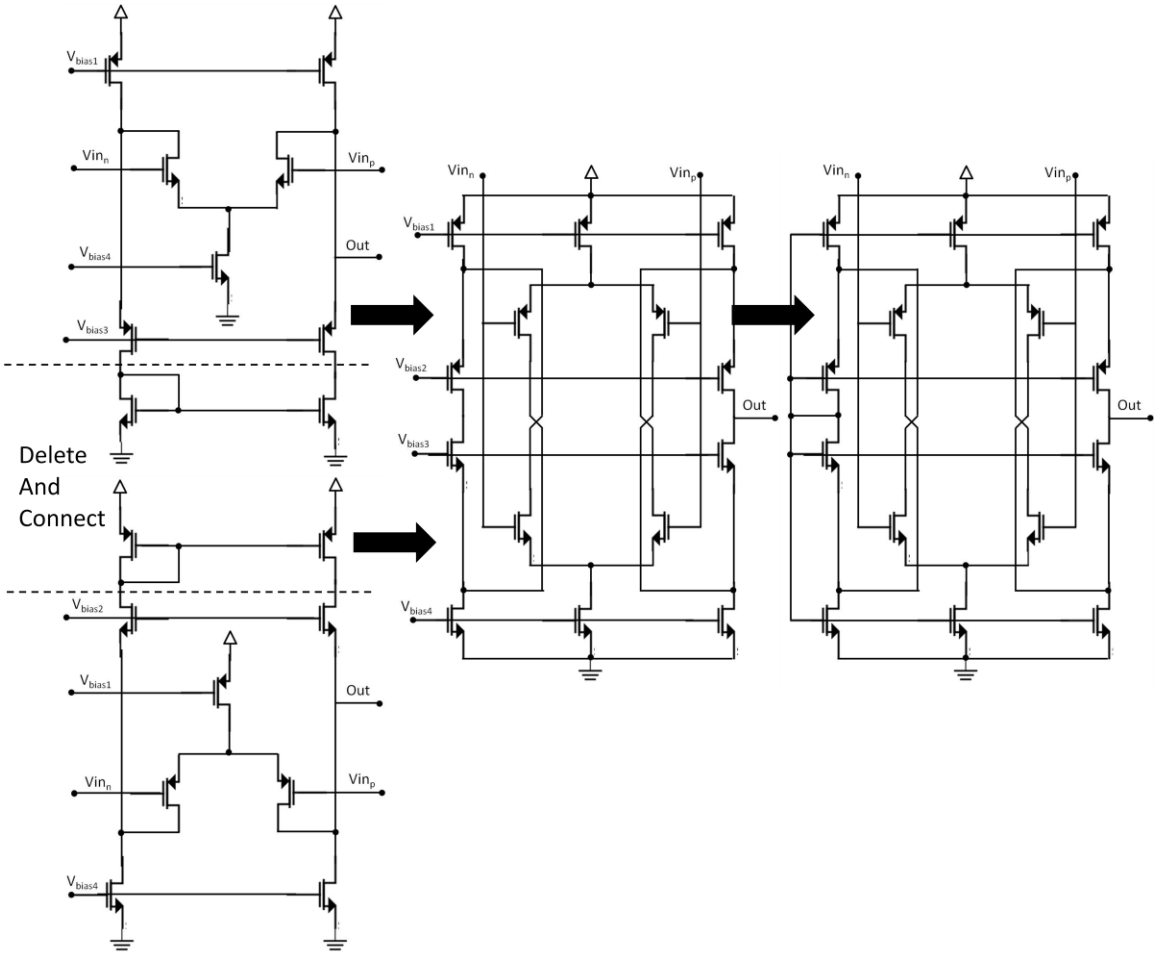

Figure 6: The Design Process of Self-Biased VCDA [24]

To correct this issue, Abdelmoneum et al. [25] suggested a new technique to create a self biased folded cascode amplifier without taking up the second output as a bias point. The idea of this technique was to create replica chains to duplicate the output devices. With proper transistor sizing, these replica chains produced an internal point with the same common mode voltage characteristics as the output nodes. These duplicate output nodes were then used to bias the transistors in the Op-Amp as shown in figure 7 [25]. However, this resulted in a decrease in the total amplifier gain as will be evident from the amplifier analysis.

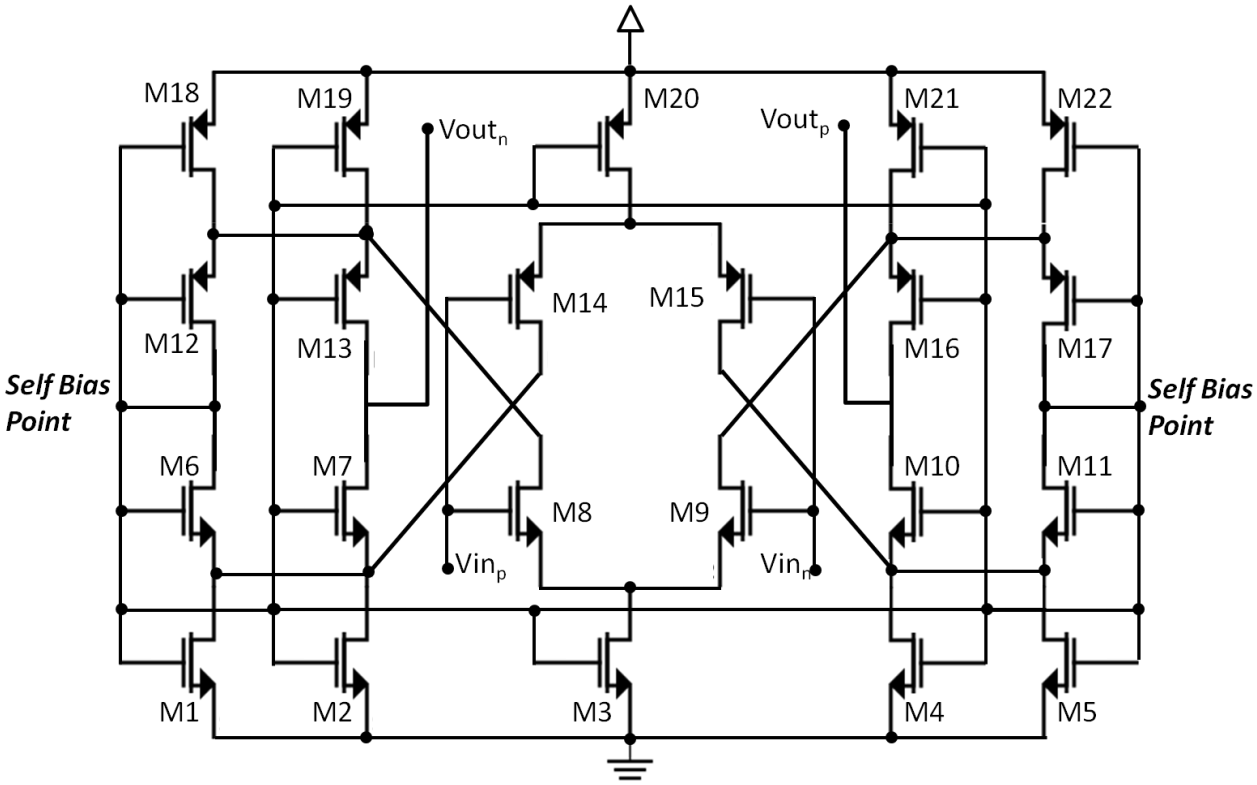

Figure 7: Folded Cascode Op-Amp with replica Chains Biasing [25]

II. Objectives

The previous discussion indicates that there are several types of amplifiers each with its suitable applications. Also, for each Op-Amp topology, there are multiple techniques to bias the devices in the Op-Amp. Consequently, the design process has to include all of these aspects in addition to the inherited property of analog circuits of non scalability between different fabrication technologies, thus making the design problem a very tedious task. In fact, the design process is sometimes considered an art that depends on the skills and experience of the circuit designer. So, this research is done to provide a mathematical model to facilitate this design process using the fully differential folded cascode Op-Amp presented by Abdelmoneum et al [25]. The model will be verified by simulations using different technologies to make sure that it is valid over a wide range of device sizes and fabrication processes. However, with the continuous shrinking of the transistor size, this model will only provide a fast technique to approximate the behavior of the circuit which will nevertheless help the designer to reach his/her design goals efficiently without going too much into trial and error during the design phase.

III. Folded Cascode Amplifier Characterization and Derivation Technique

The procedure for this research has two main parts. The first part is to provide the reason for using the replica chain biasing technique and the folded cascode fully differential self biased amplifier. This section is mainly about proving the usefulness and superiority of this amplifier along with its self biasing technique. The second part is mainly the derivation of design equations for the amplifier.

A. Merits of Replica Chain Biasing and Folded Cascode Fully Differential Self Biased Amplifier

The main idea behind the replica chain biasing is that by duplicating the output devices, every change that may occur at the output devices will be replicated to the bias devices thus the bias point will follow the changes in the output devices. The self biasing technique helps significantly reduce the bias point variations due process variations, and temperature drift. This is because the replica devices will be laid out near the original output devices ;therefore, they will go through similar or nearly equivalent process variations as well as similar or nearly equivalent temperature drift. To prove this, Abdelmoneum et al. [25], constructed the folded cascode fully

differential self biased amplifier and proved that the replica chains are a very viable self biased solution.

To demonstrate the usefulness of the replica chain biasing technique, Abdelsalam et al. [26], designed another self biased amplifier using the same biasing technique. Figure 8 shows the designed amplifier. Due to the application requirements, compensation using C1 and C2 was utilized to enhance the amplifier's phase margin to guarantee amplifier stability. Also, single ended input was required; so, one of the input ports was tied to the internal biasing point.

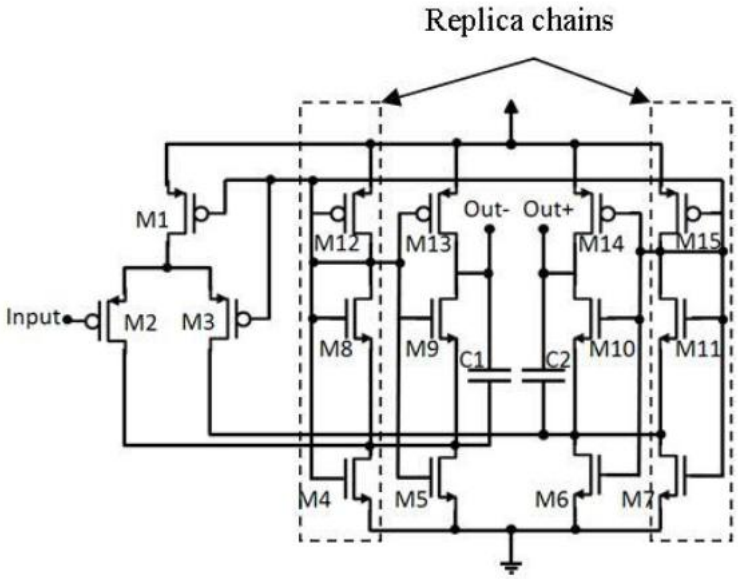

Figure 8: Self biased folded cascode operational amplifier [26]

This amplifier was then used to construct an oscillator to support on chip MEMS sensors and devices. The oscillator was constructed from the following blocks: a variable gain amplifier, on chip MEMs resonator, gain control circuitry, envelop detector and a comparator as shown in Figure 9.

To properly operate the oscillator, the amplifier should have a large gain at the start in order to be able to grow the oscillation. Then, when the oscillation magnitude reaches a predefined level, the amplifier gain has to be lowered such that it matches the losses around the feedback loop thus keeping the loop gain unity and oscillation stability. These losses come usually from the damping factors of the resonator and the rest of oscillator components.

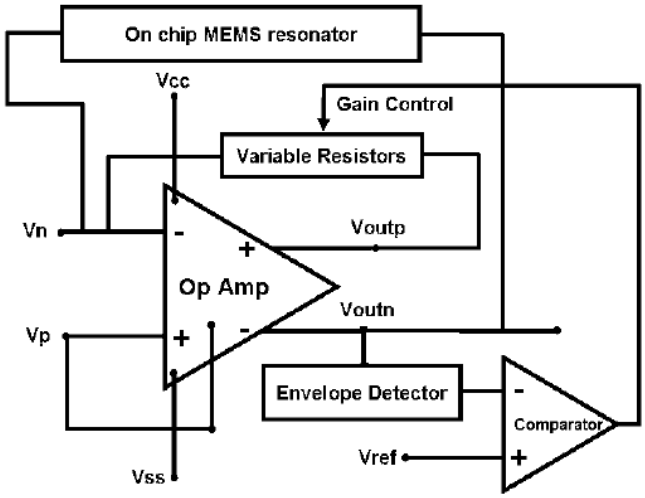

Figure 9: General Topology of the Series Resonant Vibrating Capacitive Micro Electro Mechanical Resonator Oscillator. [26]

The variable gain operating condition, required for the correct functionality of the oscillator, mandates that the operating point of the amplifier have to change in accordance with the gain. Varying the amplifier gain can be achieved through changing the feedback loop gain to accommodate the requirement for each oscillation stage. This makes this application very suitable to test the idea of replica chain biasing. Furthermore, the compensation capacitors at the outputs helped setting the

phase margin of the amplifier within acceptable range during different operation modes. Figure 10 shows a time domain simulation for the described oscillator system.

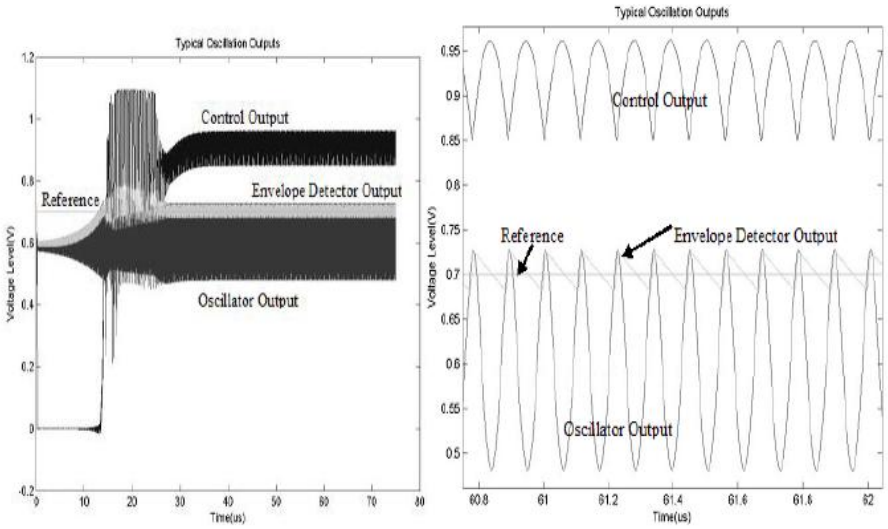

Figure 10: Oscillator output at typical corner showing oscillation build up and sustained oscillations [26]

Figure 10 clarifies the oscillator operation. In the first stage the amplifier has a very high gain such that oscillation can be achieved and grown. After the oscillation magnitude reaches a specified reference level, the amplifier gain is lowered such that the oscillation is maintained. The discussed amplifier and oscillator design were tested against analog process variation and temperature drift. The oscillator managed to operate across a very wide range of temperatures from -10°C to 110°C and across all analog process skew corners. Therefore, it can be concluded that the replica chain self biasing technique is a robust method to bias analog amplifiers.

In addition, to further prove the superiority of amplifiers designed in [25], the amplifier was characterized before the mathematical formulation

was derived. Several amplifier characteristics were extracted as will be discussed in the following paragraphs.

Common Mode Rejection Ratio (CMRR)

The CMRR is a very important amplifier characteristic that determines the ability of the amplifier to reject common signals on its input ports. This becomes vital if the amplifier is expected to operate in an area with a lot of signal noise superimposed on the signal that is supposed to be amplified. Because of the spatial proximity of the input devices, it can be assumed that both the input ports will have almost equal noise signals and the amplifier has to reject this common signal that is superimposed on the desired signal on both inputs while in the same time providing the appropriate gain for the desired signal.

To obtain the CMRR, the amplifier was connected in the common mode input configuration and the ratio between the differential gain and the common mode gain is measured across the frequency range of simulation. Figure 11 shows the results of this simulation from which the CMRR is measured to be equal to 62dB which is high compared to other amplifier topologies; thus giving the amplifier a sufficient common mode noise immunity.

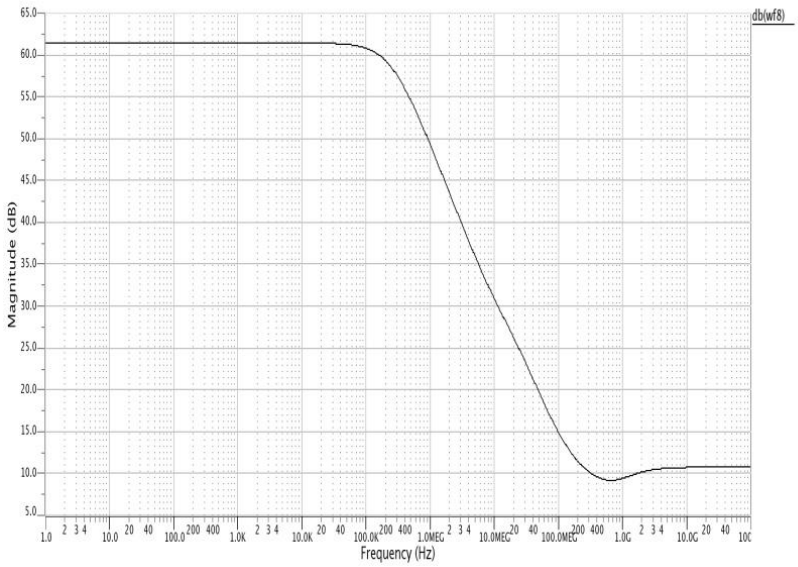

Figure 11: CMRR for the Folded Cascode Fully Differential Self Biased Amplifier

Power Supply Rejection Ratio (PSRR)

Similar to the CMRR, the PSRR describes the amplifier's ability to reject noise superimposed on its supply voltage. The power supply noise is very common in analog circuit due to signal interference from external signal sources or if the same supply is used in any other circuit block, noise can propagate from circuit block to the other. So, it is very critical for an amplifier to have as high PSRR as possible to eliminate such noise. To measure the PSRR, shown in Figure 12, the input ports were connected to a DC voltage source corresponding to the common mode of the input signal while the power supply was represented by a small signal AC voltage source having a DC level of the desired power supply. The PSRR can then be calculated by evaluating the ratio between the amplifier differential gain and

the gain of the power supply variations. This was calculated to be 48.7 dB which is considered a high rejection ratio which is desired in many applications.

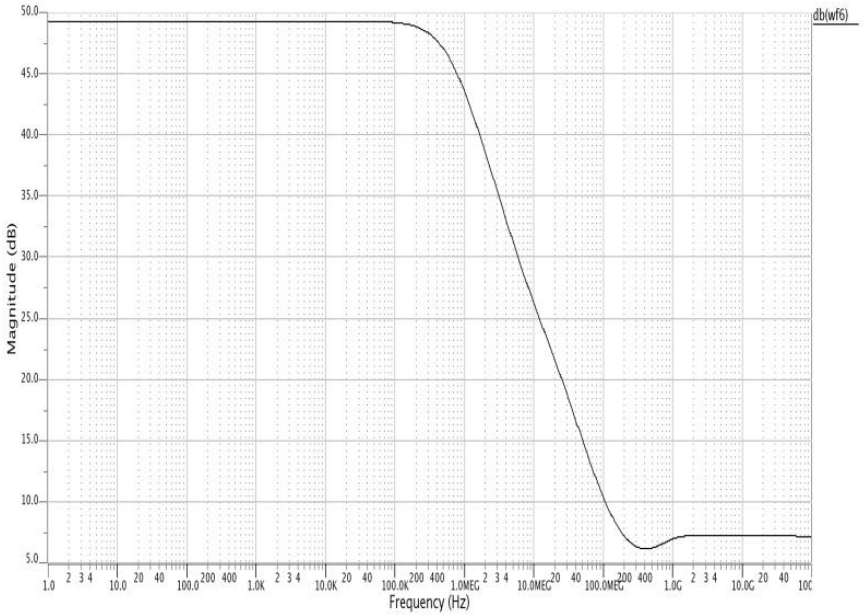

Figure 12: PSRR for the Folded Cascode Fully Differential Self Biased Amplifier

Common Mode Range (CMR)

The CMR is basically the range of input bias points that can be used with the amplifier having almost the same performance. This is a desirable trait for an amplifier if it is required to be as generic as possible to be able to achieve the required function regardless of the input voltage. This was obtained by sweeping the input common mode value and measuring the DC differential gain at each common mode voltage. It can be noted from Figure 13 that this type of amplifiers has a very narrow CMR. This is due to the self

bias nature of this topology. Being self biased makes the transistors operation depends on the operating point of the circuits thus giving a narrow common mode range.

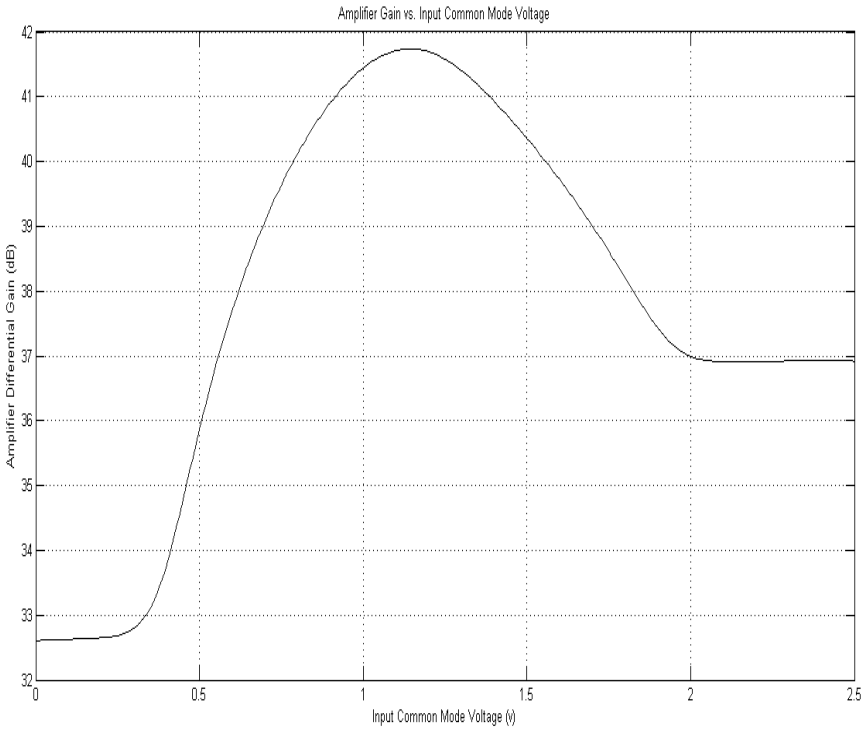

Figure 13: Input Common Mode Range (CMR)

Input and Output Impedances

The input impedance was measured by measuring the ratio between the input voltage and input current during the frequency domain simulation. This resulted in input impedance in the range of 10^{10} Ohm which is a desired property for voltage amplifiers. To measure the output impedance of the amplifier, the inputs were connected to a DC source corresponding to the

desired common mode voltage and a test source was connected to the output port. The single ended output impedance was then simply calculated by dividing the test voltage over the test current as shown in Figure 14. From Figure 14, it can be noted that the output impedance is much smaller than input impedance which is desired when designing a voltage amplifier.

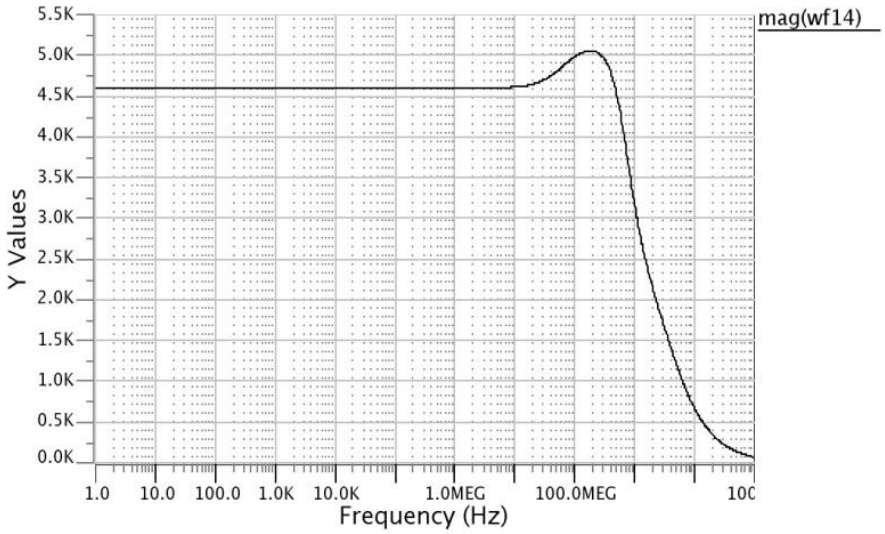

Figure 14: Output Impedance of the Amplifier

Settling Time and Slew

The settling time describes the time needed for the amplifier to reach its desired output while the slew rate describes how fast the amplifier reaches such level. To measure the settling time and slew rate, a voltage step is applied to the input and the single ended output is observed. From Figure 15, the settling time is measured to be 1.117ns and the slew rate is measured to be 1.695×10^{9} V/s. These are very reasonable values for the settling time

and slew rate on the process technology used to simulate this (TSMC 250nm).

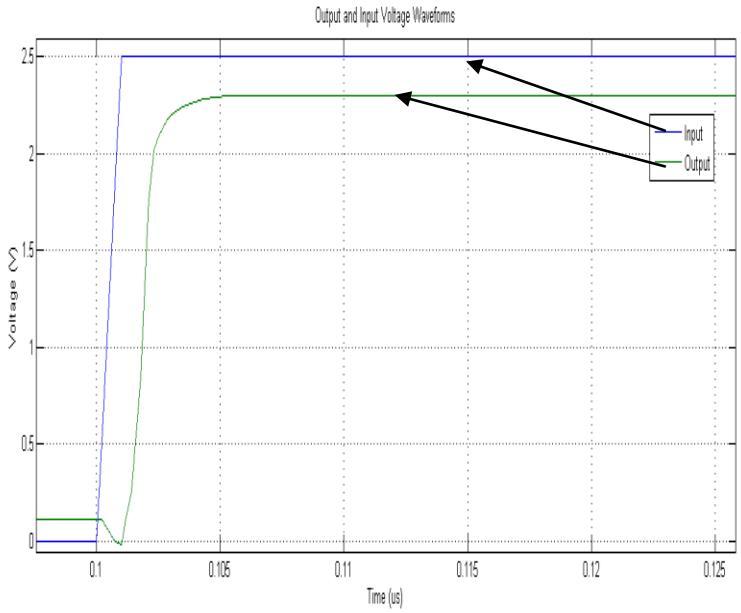

Figure 15: Single Output Waveform Corresponding to a Step Voltage Input

Temperature Drift

Finally, to make sure that this amplifier topology can tolerate temperature drift, the simulation temperature is varied across a wide range of 120°C. Figure 16 shows that due to temperature drift, the percentage change in output common mode voltage is 1.6% which is very reasonable and acceptable for this wide temperature range.

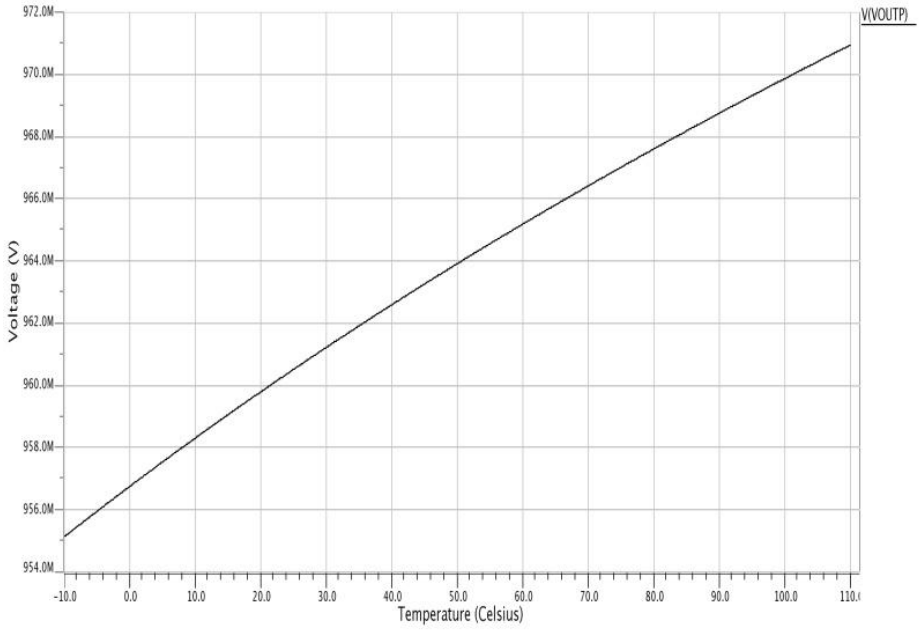

Figure 16: Output Operating Point Variation due to Temperature Drift

From the previous discussion, it is noted that the folded cascode fully differential self biased amplifier is very useful and has many desirable characteristics that make it a viable option in designing analog circuits.

B. Derivation of the Amplifier Design Equations

The second part of this research is to obtain the design equations describing the amplifier performance in terms of gain and bandwidth. This part consists of two main stages: the first stage is to provide a general technique to derive equations for the gain and bandwidth for a general complementary fully differential amplifier. The second stage is to apply this

technique to the folded cascode fully differential self biased amplifier to get its gain and bandwidth design equations and to verify the results of such equations using circuit simulations.

Stage 1: Amplifier General Mathematical Modeling Technique

From the previous discussion, we saw that all the amplifiers used to solve many design problems have the following characteristics. First, they are complementary. This means that the amplifier has both the device and its dual. For example, the input stage has both NMOS pair and PMOS pair. This increases the dynamic range of the amplifier operation because when the signal exceeds the operating range of one device, its dual will be functioning properly. Second, they are differential amplifiers. This gives the amplifier topology more noise immunity and more differential mode operating range. Consequently, this technique will analyze the family of fully differential complementary amplifiers.

To get the gain and bandwidth, the derivation technique goes through two steps. Step one is used to obtain the output resistance of the amplifier while step two is used to obtain the overall transconductance of the amplifier. These two pieces information, besides information about the dominant capacitance, can be used to get the overall amplifier gain and bandwidth. Step one starts with getting the half circuit model for the amplifier. Basically, the half circuit model means to analyze only half of the circuit. This is only enabled by the symmetry of the amplifier design, thus making the analysis procedure for the positive input similar to the analysis procedure for the negative input. Utilizing the half circuit mode will make

further circuit simplifications easier. Next, input devices, bias devices and tail current devices are replaced by their equivalent output resistance (r_o). This can be done because these devices are connected to AC signal ground, thus deactivating the transistor's current sourcing capabilities and making the device a simple resistance. If the amplifier design contains any diode connected devices, they can be replaced by their equivalent resistance. This equivalent resistance is basically the device output resistance in parallel with the inverse of the device transconductance. In most cases, the device output resistance is much greater than the inverse of the transconductance. Thus, the equivalent resistance of a diode connected device can be simplified to be the inverse of the device transconductance. All of these resistances can be combined into only one larger resistance connected in parallel to the output devices. Due to the complementary nature of the amplifiers under investigation, this large resistance can be divided into two resistances: the first is associated with the NMOS output device and the other is associated with the PMOS output device. This division has to take the relative driving strength of the PMOS and NMOS devices into consideration. Next, each output branch can then be treated as common source amplifier with degeneration resistor for which the output resistance can be easily calculated. Finally, the two output resistances for the two common source amplifiers are combined in parallel to get the overall output resistance for the amplifier. Figure 17 describes this process.

The second step is used to obtain formulation for the overall amplifier transconductance. It starts with obtaining the half circuit model for the amplifier. Next, each device is replaced with its equivalent model. In this case, the input devices are replaced with voltage controlled current sources

parallel with their output resistance. All other transistors are treated exactly as was done while calculating output resistance. After doing the necessary simplifications, the total current flowing in the output branch due to the input devices is then calculated. This is done using the current dividers and superposition principles. Finally, the transconductance can be obtained by dividing the overall current in the output branch over the total input voltage applied to the input devices. This process is illustrated by Figure 18.

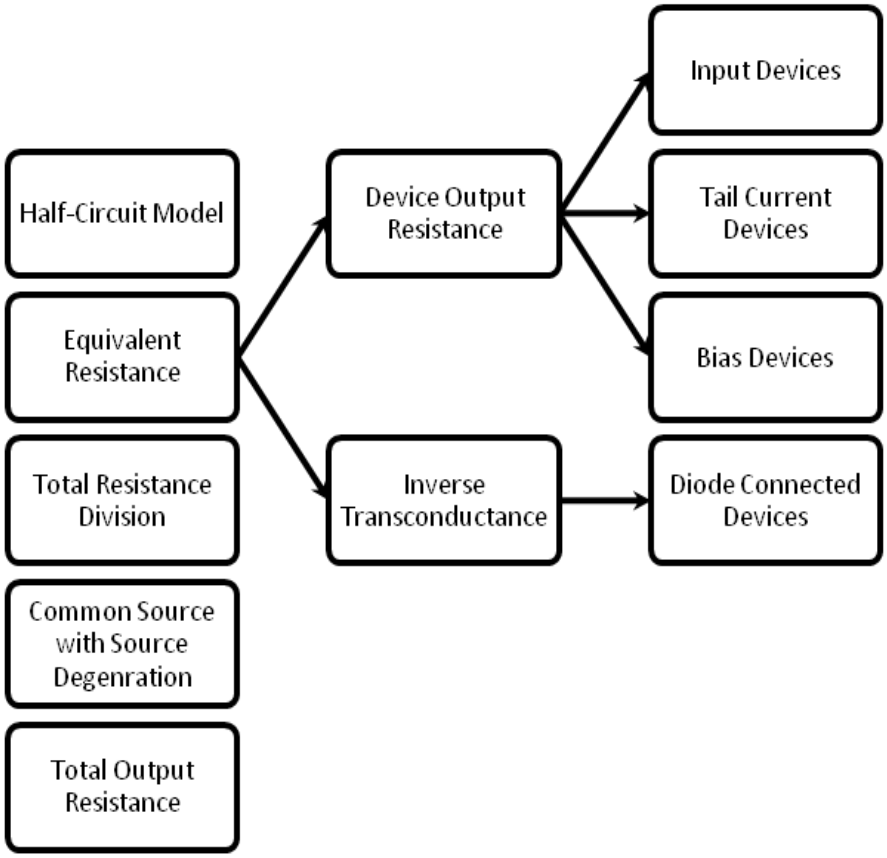

Figure 17: Steps for Obtaining Formulation for the Amplifier Output Resistance

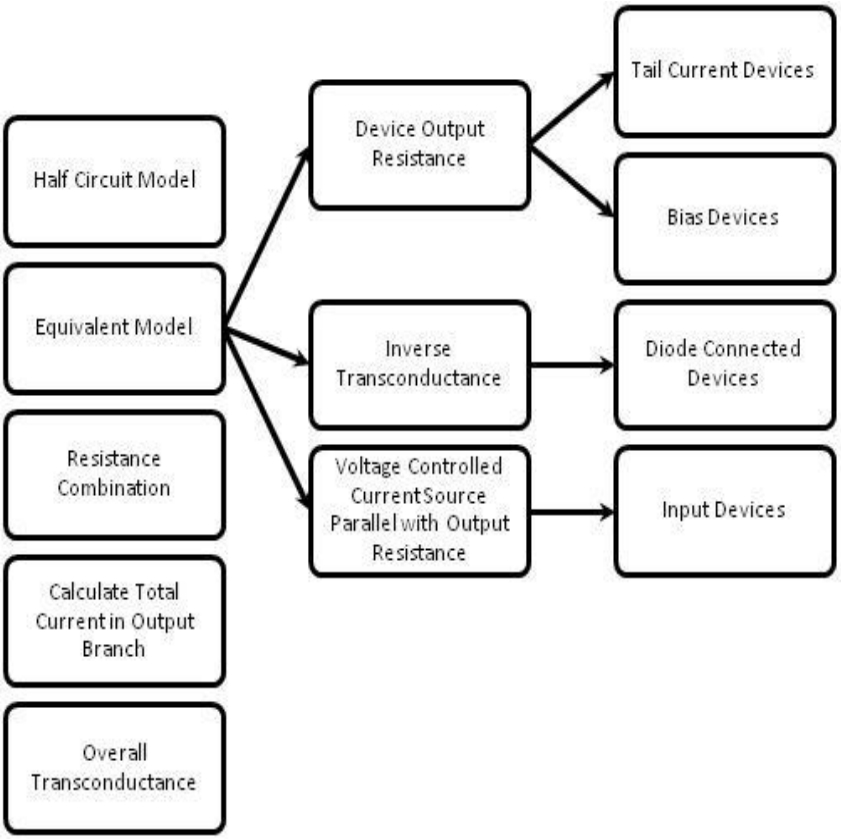

Figure 18: Steps for Obtaining Formulation for the Amplifier Overall Transconductance

In order to get the overall amplifier gain, the expressions for the amplifier output resistance and overall transconductance are multiplied. As for the bandwidth, the total output resistance expression can be used along with the information about the total dominant capacitance for the amplifier to obtain a detailed expression for the amplifier bandwidth.

Stage 2: Mathematical Modeling Procedure for the Folded Cascode Fully Differential Self Biased Amplifier

After discussing the general algorithm to obtain expressions for the amplifier gain and bandwidth, it will be applied to the folded cascode fully differential self biased amplifier. To compare the difficulty of the proposed scheme versus the direct modeling technique, the direct modeling technique is described briefly. It starts using the small signal model for the transistors shown in figure 19 to derive equations for the gain and output resistance of the amplifier. This model includes the effects of the ideal transistor, the channel length modulation, and the body effect. However, the body effect is out of scope of this work and hence it won't be included in upcoming analyses.

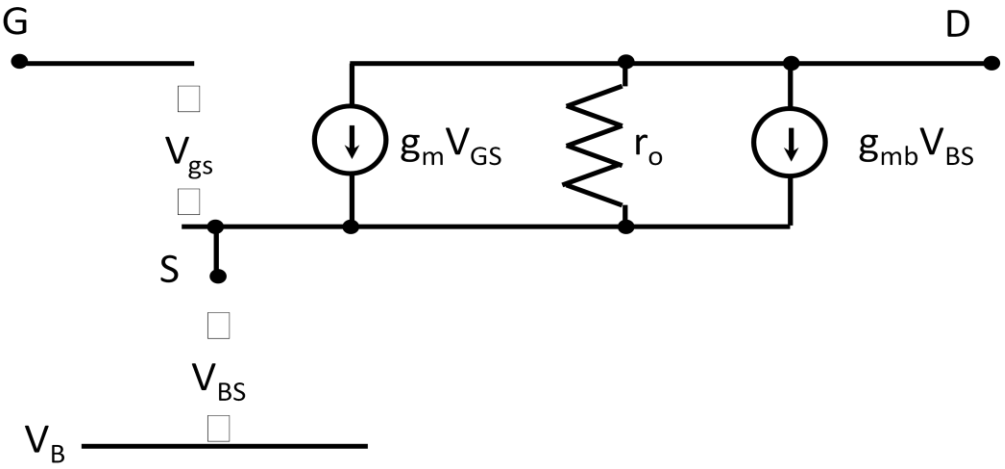

Figure 19: Small Signal Transistor Model [1]

This model can be used to replace all the transistors in the folded cascode amplifier and the interactions between the different devices were analyzed. This model enabled the use of basic circuit analysis techniques to

calculate the gain and output resistance of the amplifier. In order to derive the frequency response for the circuit, this model can be updated to include the device parasitic capacitances. These parasitic capacitances are represented by a lumped capacitor element between the terminals with such parasitic components.

However, using the transistor model introduced in Figure 19 will produce a very complicated model for the overall Op-Amp since there are 22 devices in the circuit. Consequently, the new proposed technique is used to get the amplifier's design equations. Following the steps outlined in the previous discussion, the model went through a series of simplifications that facilitated the process of finding the required parameters.

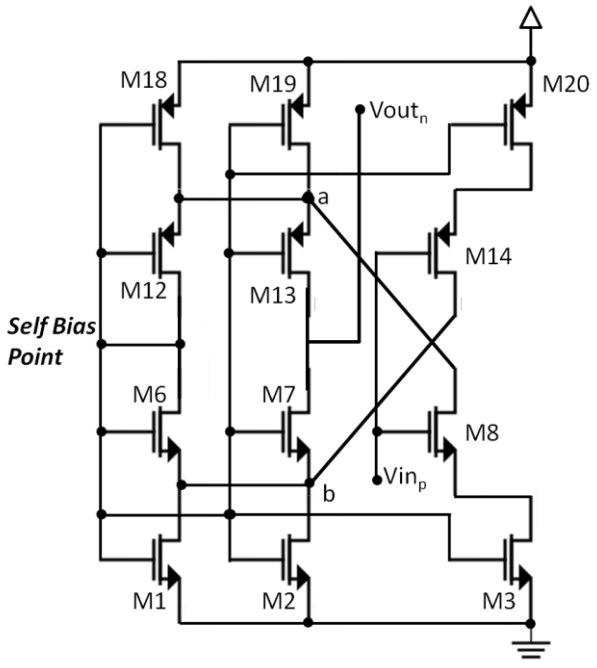

Figure 20: Half Circuit Model for the Fully Differential Self Biased Folded Cascode Op-Amp

Figure 20 shows the half circuit simplification for the folded cascode Op-Amp. It will be used to get the overall trans-conductance (G_m) of the amplifier and the overall Op-Amp output resistance (R_{out}). The overall circuit differential gain is simply twice the multiplication of these two quantities $A_v=2G_m\cdot R_{out}$. The factor 2 is introduced because only half of the circuit was analyzed using the half circuit model.

To get the output resistance of the amplifier, the AC input signal (V_{in}) is disabled (AC ground) and resistance seen from the output port is calculated. Starting from the half circuit model outlined in Figure 20 in addition to assuming the bias point can be considered an AC signal ground (this will be verified though simulations), the resistance at point '**a**' of transistors M18, M19, and M8 can be represented by their output resistance r_0. The main advantage of the previous assumption (bias point is ac signal ground) is that it can simplify the analysis procedure through deactivating the internal current sources of the bias transistors; thus, a transistor can be represented by its output resistance only. These resistors can then be combined in parallel to get the resistance 'R_A' at the folding point '**a**'. The same can be done to transistors M1, M2, and M14 to calculate the resistance 'R_B' at point '**b**'. Next, each of the diode connected transistors M6 and M12 can be modeled by the parallel combination of their output resistance and the inverse of their transconductance 'R_{nd}' and 'R_{pd}', respectively.

After that, it can be noted that R_A and R_B can be combined in series as well as R_{nd} and R_{pd}. These equivalent resistors can be combined in parallel to get the total resistance seen between points '**a**', and '**b**'.

Finally, this total resistance can be divided into two degenerative source resistances in series with the two output transistors M7 and M13. The relative current driving capabilities of NMOS and PMOS have to be taken into consideration such that the weaker device is connected to the higher resistance and vice versa. By doing this, the total amplifier output resistance is the parallel combination of the resistances seen from a common source stage with a degenerative source resistance. This process is depicted in Figure 21.

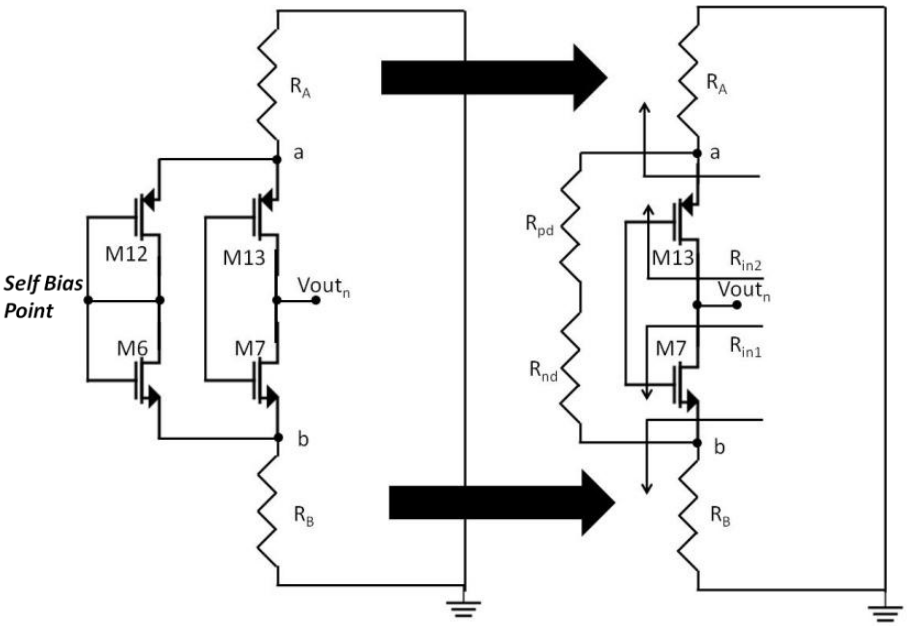

Figure 21: Simplification Steps for Output Resistance Calculation

Next, using the proposed simplification technique, as shown in Figure 22, the overall transconductance of the amplifier can be obtained as follows.

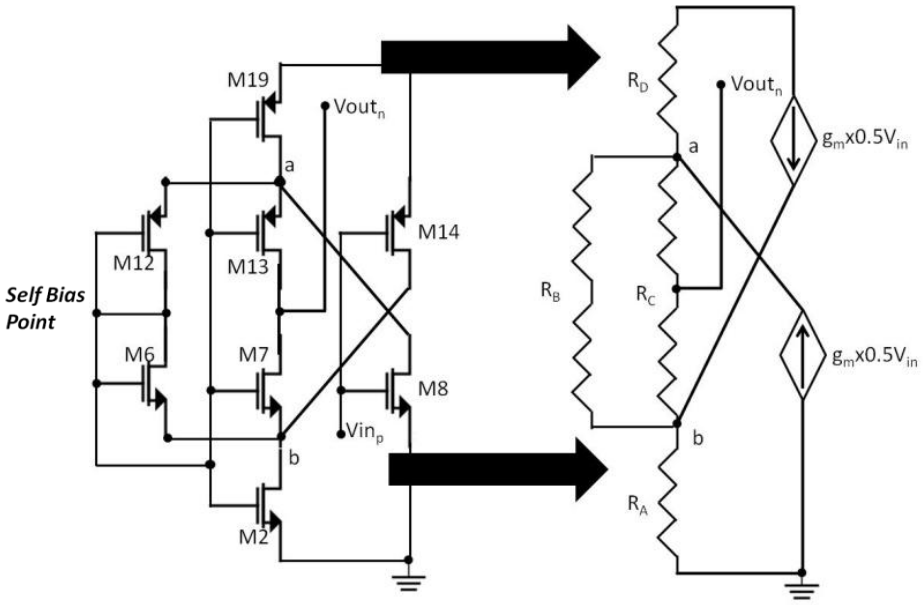

Figure 22: Simplification Steps for Transconductance Calculations

To get the amplifier total transconductance, the input devices M8 and M14 are replaced with their small signal model (voltage controlled current source) and the electrical current at the output branch is calculated relative to the input voltage. The same assumption of considering the bias signal as AC signal ground is used. This is valid because achieving amplification requires that most of the signal is transmitted through the output devices not to the diode connected bias transistors. At point '**a**', the output resistances of devices M18, M19, and M8 are combined in parallel to produce R_D. Similarly, the output resistances of devices M1, M2, and M14 can be combined to produce R_A.

Next the resistances seen across the two diode connected transistors, M6, and M12, are combined in series to get the total resistance of the branch '**B**'. After this, the output devices, M7 and M13, are replaced by their

equivalent resistance. This is simply the resistance seen from the source of a common gate amplifier which is the parallel combination of the output resistance and the inverse of the transconductance of the MOS transistor. The resistance of branch '**C**' is simply the series combination of the two common gate amplifier output resistances.

Finally, using the superposition and current division principles, the total current in the output branch can be calculated. Hence, the overall transconductance is simply the ratio of this current to the input voltage.

Next, the frequency response is analyzed. A simple method to get the frequency response is to assume that there is a pole associated with every node in the circuit where both a capacitor and a resistor are assumed to be connected. In this Op-Amp circuit, one can note that there are two poles: one at the folding node and another at the output node with the pole at the output node being dominant [19]. Consequently, the bandwidth of the circuit can be obtained by calculating the value of this dominant pole which can be determined from the time constant at this point. Thus, at the output node, the time constant is the multiplication of the output resistance calculated in the previous part and the total capacitance seen at this node which is the total capacitance seen from the drain terminals of both the output devices.

After getting the mathematical model, it has to be verified using circuit simulation. Here, the Op-Amp was implemented on a circuit simulator and different simulations were run to verify the results derived from the theoretical analysis. These simulations included DC operating point simulation, time domain simulations, and frequency response simulations. The DC operating point was used to get the device parameters for each

transistor to be plugged into the theoretical equations. The time domain analysis showed how the circuit behaves in real time which can be used to determine the value of the gain. The frequency response enabled the measurement of bandwidth, gain, and system poles and zeros to estimate the transfer function. These simulations were run at different operating points and with different device sizes across three different fabrication processes (TSMC 180nm, 250nm , and 350nm) then the measurement results were compared to the values obtained from the mathematical model derived previously.

IV. Amplifier Modeling Results

A. Amplifier Mathematical Model

As discussed, the derivation for the mathematical Model went through two stages to derive and verify the mathematical formulation for the folded cascode self biased amplifier. The first stage was to get the theoretical analysis for the Op-Amp parameters. Using the new proposed circuit simplification technique for the complementary differential amplifiers, the gain and bandwidth equations for the folded cascode fully differential self biased amplifier were obtained.

First, to get the output resistance of the amplifier, the AC input signal (V_{in}) is disabled (AC ground) and resistance seen from the output port is calculated. The resistance at point '**a**' was represented by the output

resistances 'r_0' of transistors M18, M19, and M8. These resistors were combined in parallel to get the total resistance at the folding point '**a**' as described by the following Equation 1:

$$R_A = r_{o,M18} \parallel r_{o,M19} \parallel r_{o,M8} \qquad (1)$$

where:

- r_o is the output resistance of the transistor

The same simplification was performed for transistors M1, M2, and M14 to calculate the resistance at point '**b**' as described by Equation 2:

$$R_B = r_{o,M1} \parallel r_{o,M2} \parallel r_{o,M14} \qquad (2)$$

Next, each of diode connected transistors M6 and M12 were modeled by the parallel combination of their output resistance and the inverse of their transconductance as described by Equations 3, and 4.

$$R_{pd} = \frac{1}{g_{m,M12}} \parallel r_{o,M12} \qquad (3)$$

$$R_{nd} = \frac{1}{g_{m,M6}} \parallel r_{o,M6} \qquad (4)$$

where:

- g_m is the transconductance of the transistor

After that, 'R_A' and 'R_B' were combined in series as well as 'R_{nd}' and 'R_{pd}'. These equivalent resistors were then combined in parallel to get the total resistance seen between points '**a**', and '**b**' and Equation 5:

$$R = (R_{pd} + R_{nd}) \parallel (R_A + R_B) \qquad (5)$$

Finally, the total resistance, described by Equation 5, was divided into two degenerative source resistances in series with the two output transistors M7 and M13. The relative current driving capabilities of NMOS and PMOS have to be taken into consideration such that the weaker device is connected to the higher resistance and vice versa. By doing this, the total amplifier output resistance is the parallel combination of the resistances seen from a common source stage with a degenerative source resistance as described by Equations 6, 7, and 8:

$$R_{in1} = [1 + g_{m,M7} r_{o,M7}] NR + r_{o,M7} \qquad (6)$$

$$R_{in2} = [1 + g_{m,M13} r_{o,M13}](1 - N)R + r_{o,M13} \qquad (7)$$

$$R_{out} = R_{in1} \parallel R_{in2} \qquad (8)$$

$$N = \frac{\mu_p W_p}{\mu_n W_n + \mu_p W_p} \qquad (9)$$

where:

- N is a constant that represents the relative driving capabilities of the PMOS to NMOS device and it is used to divide the total resistance obtained in Equation 5

Second, the overall amplifier transconductance was obtained as follows. Using the simplifications outlined in Figure 22, the overall

transconductance of the amplifier can be obtained as follows. The input devices M8 and M14 were replaced with their small signal model (voltage controlled current source) and the electrical current at the output branch is calculated relative to the input voltage. At point '**a**', the output resistances of devices M18, M19, and M8 were combined in parallel to produce 'R_D' as described by Equation 10:

$$R_D = r_{o,M18} \parallel r_{o,M19} \parallel r_{o,M8} \qquad (10)$$

Similarly, the output resistances of devices M1, M2, and M14 were combined to produce 'R_A' as described by Equation 11:

$$R_A = r_{o,M1} \parallel r_{o,M2} \parallel r_{o,M14} \qquad (11)$$

Next the resistances seen across the two diode connected transistors, M6, and M12, were combined in series to get the total resistance of the branch '**B**' as described by Equation 12:

$$R_B = \left(\frac{1}{g_{m,M6}} \parallel r_{o,M6} \right) + \left(\frac{1}{g_{m,M12}} \parallel r_{o,M12} \right) \qquad (12)$$

After this, the output devices, M7 and M13, were replaced by their equivalent resistances which were determined to be the parallel combination of the output resistance and the inverse of the transconductance of the MOS transistor. The resistance of branch '**C**' was calculated as the series

combination of the two common gate amplifier output resistances as described by Equation 13.

$$R_C = \left(\frac{1}{g_{m,M7}} \| r_{o,M7} \right) + \left(\frac{1}{g_{m,M13}} \| r_{o,M13} \right) \qquad (13)$$

Finally, using superposition and current division principles, the total current in the output branch was calculated. Then, the overall transconductance was obtained by Equation 14.

$$G_m = CR_B \qquad (14)$$

$$C = \frac{R_A g_{m,M14}}{R} + \frac{R_D g_{m,M8}}{R} \qquad (15)$$

$$R = (R_B + R_C)(R_A + R_D + R_B \| R_C) \qquad (16)$$

Third, the frequency response was analyzed. To calculate the amplifier bandwidth, the time constant needs to be evaluated at the output node. To obtain this time constant, the total capacitance at the output node was calculated using Equation 17. Then, the time constant was obtained by the multiplication of the output resistance, calculated in the previous part and, the total capacitance seen at the output node.

$$C_{out} = C_D\big|_{NMOS} + C_D\big|_{PMOS} \qquad (17)$$

$$C_D = C_{JSW} * (W + 2L_D) + C_J * L_D * W + C_{JSWG} * W \qquad (18)$$

where:

- C_D is the capacitance seen from the drain terminal
- C_{JSW} is the junction capacitance per unit length for the drain sidewalls.
- C_J is the device junction capacitance per unit area
- C_{JSWG} is the junction capacitance per unit length for the drain side that is facing the channel

However, one should note that these junction capacitances are affected by the body to source voltage. These effects were not included to design for the worst case capacitance obtained when there is no voltage difference between the source and body. Consequently, the calculated bandwidth numbers are always lower than the simulated ones. Then, using the information about 'R_{out}', the bandwidth was calculated using the following equation:

$$BW = 1 / (2 \pi R_{out} C_{out}) \qquad (19)$$

B. Simplifications, and Special Cases

As can be noted from the previous discussion, the equations for the amplifier output resistance and overall transconductance are very complicated. Consequently, a series of simplifications were carried out in order to represent them in a more convenient form. The output resistance will be simplified first then the overall transconductance. First, transistors M18 and M19 as well as transistors M1 and M2 are connected completely in parallel and they are sized equally. Consequently, only one of them can be

considered after doubling its driving capabilities thus dividing its output resistance by 2 and multiplying its transconductance by 2. Furthermore, the output resistance of the input devices, M8 and M14, are much larger than these of the bias devices, M1, M2, M18, and M19. This is because the bias devices have to carry larger amounts of currents in order to correctly bias the amplifier devices. Therefore, Equation 1 and Equation 2 can be reduced to Equation 19 and Equation 20.

$$R_B = \frac{r_{o,M1}}{2} \qquad (19)$$

$$R_A = \frac{r_{o,M18}}{2} \qquad (20)$$

As for the diode connected devices, the output resistance is much larger than the inverse of the device transconductance and thus it can be ignored. The reason for that these diode connected devices are replicas of the amplifier output devices. Usually, output devices are required to have large transconductance values to achieve amplifier high gain requirements. Thus, the inverse transconductance is very small compared to the device output resistance. Therefore, Equations 3, and 4 can be rewritten as Equations 21, and 22, respectively.

$$R_{pd} = \frac{1}{g_{m,M12}} \qquad (21)$$

$$R_{nd} = \frac{1}{g_{m,M6}} \qquad (22)$$

Finally, Equation 6 and Equation 7 describe the total resistance output resistance of a common source amplifier with source degeneration resistor. Usually, the term $g_m r_o$ is usually much greater than unity because this term is directly related to device gain which a very high value is giving the fact that we are analyzing the amplifier output stage devices. Therefore, Equations 6 and Equation 7 can be rewritten as Equation 23 and Equation 24

$$R_{in1} = \lfloor g_{m,M7} NR + 1 \rfloor r_{o,M7} \qquad (23)$$

$$R_{in2} = \lfloor g_{m,M13}(1-N)R + 1 \rfloor r_{o,M13} \qquad (24)$$

$$R_{out} = R_{in1} \parallel R_{in2} \qquad (25)$$

$$N = \frac{\mu_p W_p}{\mu_n W_n + \mu_p W_p} \qquad (26)$$

$$R = (R_{pd} + R_{nd}) \parallel (R_A + R_B) \qquad (27)$$

Now, the overall amplifier transconductance will be simplified. First, as mentioned earlier regarding the parallel connection of M1 and M2 as well as M18 and M19, each of these device pairs can be combined in parallel. Therefore, Equation 10 and Equation 11 can be reduced to Equation 28 and Equation 29.

$$R_A = \frac{r_{o,M1}}{2} \qquad (28)$$

$$R_D = \frac{r_{o,M19}}{2} \qquad (29)$$

Similar to the output resistance simplification, Equation 12 and Equation 13 can be reduced to Equation 30 and Equation 31 due to the fact that the device output resistance is much larger than the inverse of the device transconductance.

$$R_B = \left(\frac{1}{g_{m,M6}}\right) + \left(\frac{1}{g_{m,M12}}\right) \qquad (30)$$

$$R_C = \left(\frac{1}{g_{m,M7}}\right) + \left(\frac{1}{g_{m,M13}}\right) \qquad (31)$$

To further simplify the equations, a hypothetical special case of interest was considered. It is the case of the symmetric complementary circuit. Symmetric means that all the devices of the same type across the differential pair share the same characteristics while complementary means that the corresponding PMOS and NMOS devices have the same characteristics. Using these outlines assumptions, the following simplified expressions were obtained.

$$R_{out} = \left[\frac{1 + r_o g_m}{2 + r_o g_m}\right] r_o \qquad (32)$$

$$G_m = \frac{r_o g_m^2}{2(1 + r_o g_m)} \qquad (33)$$

$$A = 2G_m R_{out} = \frac{(r_o g_m)^2}{(2 + r_o g_m)} \qquad (34)$$

Appendix A provides the detailed derivations for the previous expressions. It can be noted that for high values of device transconductance, the total output resistance will only depend on the device output resistance itself in the case of full complementary and symmetric design. Also, this means that the total gain of the amplifier was reduced, relative to the externally biased folded cascode amplifier in order to achieve the amplifier self bias. Furthermore, It can be noted that in cases where $r_o g_m$ has a high value, the overall amplifier transconductance can be represented simply by $g_m/2$ which is the input device transconductance divided by 2. These pieces of information can be used accurately to describe the behavior of the amplifier under symmetric and complementary conditions. However, these

simple expressions for the amplifier output resistance, total transconductance and total output capacitance can be used as an initial starting point in the design process for any other case. This can significantly reduce the time needed for designing a folded cascode fully differential self biased amplifier. Also, it will help eliminate the time that could have been wasted through trial and error trying to design the amplifier according to the desired specifications.

C. Simulations Results

As discussed earlier, after going through the mathematical formulation, three types of simulations were used to verify the formulation. The first type is DC-operating point analysis to determine the device parameters to be plugged into the equations. The second type is the time domain analysis simulations to verify the correct functionality of the amplifier without clipping and non linearity issues. The final simulation type is frequency domain simulations to verify the values of the amplifier gain and bandwidth and hence the amplifier's total output capacitance. Three operating points and different transistor sizes are discussed here. The amplifier was simulated using three different fabrication processes: TSMC 180nm, 250nm, and 350nm. They were chosen to prove the validity of the formulation for different operating points and across a wide range of fabrication processes. The operating points are chosen as follows. The mid rail is used because this is usually the optimum point to work at because both NMOS and PMS devices will be active and it can give the highest

output signal dynamic range. The second operating point is at a voltage level below the mid rail value and the third operating point is at a voltage above the mid rail value to make sure that the formulation is valid across a wide range of input bias voltages. In addition, output device sizes were varied to make sure the formulation takes into consideration different device sizes. Appendix B provides a complete listing of device sizes used in the simulations. Simulations were used mainly using TSMC 250nm technology. In order to make sure that the derived model works for a range of technology nodes, the mid range operating point simulations were repeated for TSMC 350nm and TSMC 180nm fabrication technologies. Before going into details about the different simulation settings and their corresponding outputs, the assumption upon which the derivation was obtained has to be validated first. This assumption stated that the bias point does not carry AC signal and thus during the simplifications can be treated as virtual signal ground. Consequently, a time domain simulation is performed and the bias point voltage is compared against the input signal. Figure 23 shows this simulation result.

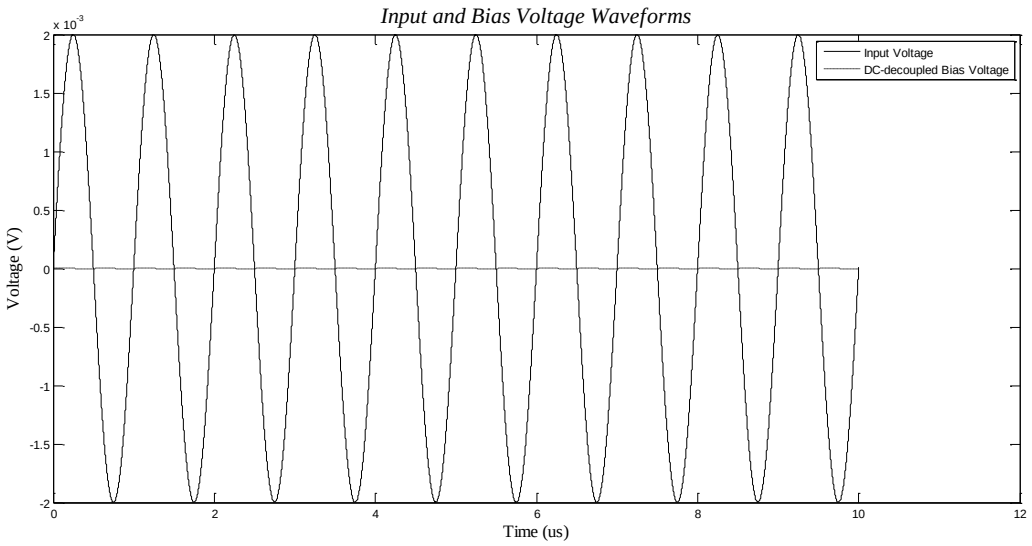

Figure 23: Input and Bias Voltages

From Figure 23, it can be concluded that the assumption used is accurate because the gain from the input signal to the bias point is equal to 2.4×10^{-4} which makes the bias point a signal ground compared to the input signal and other signals in the amplifier design.

TSMC 250nm Fabrication Technology

Mid-rail Operating point

As discussed above, three types of simulations were needed: Dc operating point, Transient time analysis, and frequency domain analysis. Table 1 shows the results of the DC operating point simulation at the mid-rail voltage operating point.

Table 1:

DC Operating Point Simulation at Mid rail operating point for TSMC 250nm Technology

Device	R_o (KOhm)	g_m
M18	8.5292	Not Required
M19	8.5292	Not Required
M8	516.1634	337.6717×10^{-6}
M1	5.9424	Not Required
M2	5.9424	Not Required
M14	5154.6	164.7986×10^{-6}
M6	856.9816	147.3794×10^{-6}
M12	3664.700	95.2081×10^{-6}
M7	856.9816	147.3794×10^{-6}
M13	3664.700	95.2081×10^{-6}

This information is then plugged into the aforementioned equations for the amplifier's total output resistance and total transconductance to obtain the results described in Table 2 and Table 3.

Table 2:

Results for Amplifier's Total Output Resistance at Mid-rail Operating Point for TSMC 250nm Technology

Quantity	Result
$\boldsymbol{R_A}$	2.9695 KOhm
$\boldsymbol{R_B}$	4.2297 KOhm
$\boldsymbol{R_{nd}}$	6.7319 KOhm

R_{pd}	10.4733 KOhm
R	5.0754 KOhm
N	0.5667
R_{in1}	1223.0908 KOhm
R_{in2}	4434.3296 KOhm
R_{out}	958.6680 KOhm

Table 3:

Results for Amplifier's Total Transconductance at the Mid-rail operating Point for TSMC 250nm Technology

Quantity	Result
R_A	2.9695 KOhm
R_B	17.2052 KOhm
R_C	17.2052 KOhm
R_D	4.2297 KOhm
R	543.7442409 MOhm
C	3.5267×10^{-9}
G_m	6.0677×10^{-5}

From the previous two tables, it was obtained that the total amplifier gain is equal to

$$A = 2G_m R_{out} = 2\times 6.0677\times 10^{-5}\times 0.9587\times 10^{6} = 116.3380 V/V = 41.29 dB$$

As for the amplifier bandwidth, Table 4 shows the details needed to get the total output capacitance.

Table 4:

Device Characteristic Capacitances for TSMC 250nm Technology

Quantity	NMOS	PMOS
Junction Capacitance (C_J)	1.752311×10^{-3}	1.894×10^{-3}
Side wall Capacitance (C_{JSW})	3.79×10^{-10}	3.12×10^{-10}
Gate Side wall Capacitance (C_{JSWG})	3.29×10^{-10}	2.5×10^{-10}
Diffusion Length (L_D)	7.98×10^{-10}	3.48×10^{-10}
C_D	3.55×10^{-15}	6.30×10^{-15}

Using the information represented in table 4, the output capacitance and the bandwidth can be obtained to be equal to

$$C_{out} = C_D\big|_{NMOS} + C_D\big|_{PMOS} = 9.85\times10-15F$$

$$BW=1/(2\pi R_{out}C_{out})=16.84\times10^{6}\ Hz$$

To verify this information, the other two simulations were run. First to validate the value for the amplifier low Frequency gain, time domain simulation is performed and the differential gain is measured. Figure 24 shows the gain to be equal to 41.58dB which lies within <1% error from the calculated value.

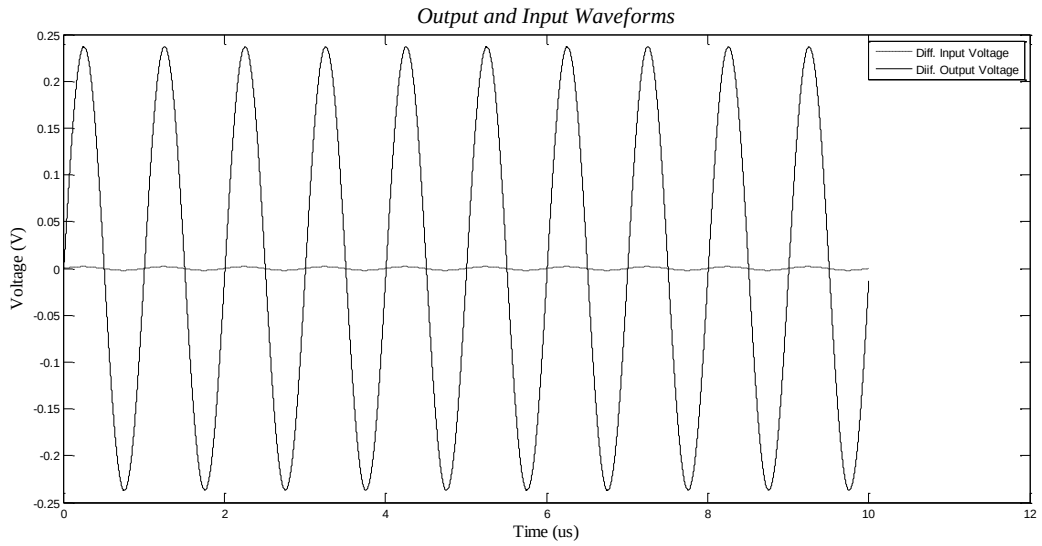

Figure 24: Time Domain Simulation at Mid-range Operating Point

Second, frequency domain simulation is performed to verify the gain and bandwidth of the amplifier. Figure 24 show the frequency domain simulation result which indicated that the bandwidth at the midrange operating point is 18 MHz. This result has an error around 6.5%. This large error due to that fact that in the bandwidth calculations the capacitances used did not take into consideration the changes due to inverse bias voltage on the device junctions. Thus, the results obtained using the equations were always lower than the values obtained from the simulations and can be considered the worst case condition for the bandwidth.

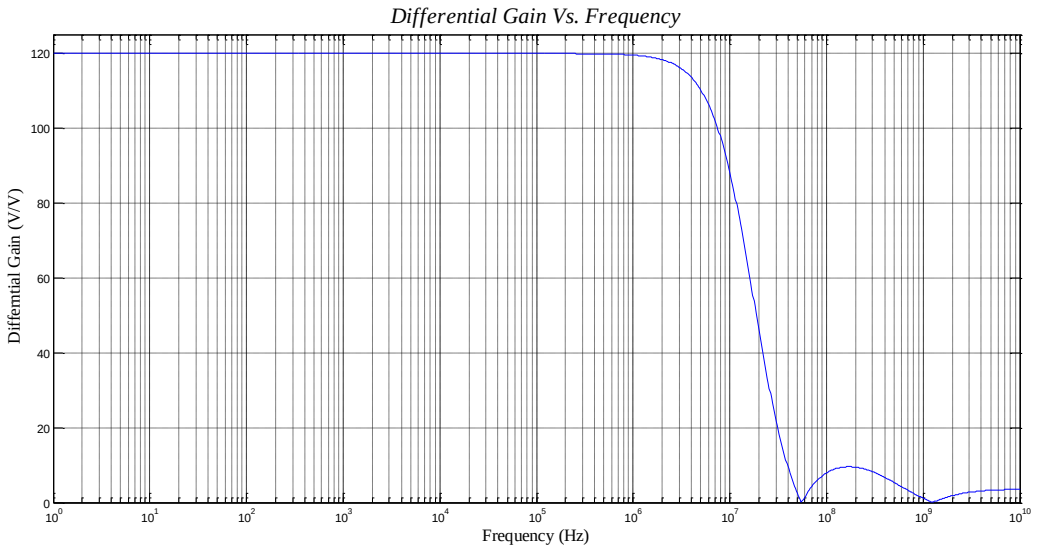

Figure 25: Frequency Simulation at the Mid-range Operating Point

1.5V Operating Point

The same steps were done for the 1.5V operating point and the results are shown in the following tables

Table 5:

DC Operating Point Simulation and 1.5V operating point for TSMC 250nm Technology

Device	R_o (KOhm)	g_m
M18	8.246	Not Required
M19	8.246	Not Required
M8	504.1398	338.0170×10^{-6}
M1	5.6797	Not Required
M2	5.6797	Not Required

M14	8379.9	123.8017×10^{-6}
M6	814.320	152.3181×10^{-6}
M12	3455.800	98.3667×10^{-6}
M7	814.3201	152.3181×10^{-6}
M13	3455.800	98.3667×10^{-6}

The information in table 5 were then used to obtained the values needed for the gain and bandwidth calculations as shown in Table 6 and 7.

Table 6:

Results for Amplifier's Total Output Resistance at 1.5V Operating Point for TSMC 250nm Technology

Quantity	Result
R_A	2.8389 KOhm
R_B	4.0896 KOhm
R_{nd}	6.5127 KOhm
R_{pd}	10.1362 KOhm
R	4.8925 KOhm
N	0.5667
R_{in1}	1160.949 KOhm
R_{in2}	4178.6563 KOhm
R_{out}	908.5327 KOhm

Table 7:

Results for Amplifier's Total Transconductance at 1.5V Operating Point for TSMC 250nm Technology

Quantity	Result
R_A	2.8388 KOhm
R_B	16.6489 KOhm
R_C	16.6489 KOhm
R_D	4.0896 KOhm
R	507.8889 MOhm
C	3.41×10^{-9}
G_m	5.68×10^{-5}

From the previous two tables, it was obtained that the total amplifier gain is equal to

$$A = 2G_m R_{out} = 2\times5.68\times10^{-5}\times0.908\times10^{6} = 103.2729V/V = 40.26dB$$

As for the amplifier bandwidth, the quantities in table 4 can be used here as well because these are technology parameters. Using the information represented in table 4, the output capacitance and the bandwidth can be obtained to be equal to

$$C_{out} = C_D\big|_{NMOS} + C_D\big|_{PMOS} = 9.85\times10^{-15}F$$

$$BW = 1/(2\pi R_{out} C_{out}) = 17.78\times10^{6}\ Hz$$

To verify this information, the other two simulations were run. First to validate the value for the amplifier low frequency gain, time domain simulation is performed and the differential gain is measured to be equal to 40.36dB which lies within <1% error from the calculated value. Second, frequency domain simulation is performed to verify the gain, and bandwidth of the amplifier. The bandwidth at the 1.5V operating point is 19MHz. This result has an error around 6.5%. As discussed earlier, this large error due to that fact that the bandwidth calculations are considered for the worst case condition.

1V Operating Point

The same steps were done for the 1V operating point and the results are shown in the following tables

Table 8:

DC Operating Point Simulation and 1V operating point for TSMC 250nm Technology

Device	R_o (KOhm)	g_m
M18	8.4556	Not Required
M19	8.4556	Not Required
M8	591.0806	303.201×10^{-6}
M1	5.9471	Not Required
M2	5.9471	Not Required
M14	3585.4	193.3893×10^{-6}
M6	853.7079	148.5631×10^{-6}

M12	3588.800	95.8142×10^{-6}
M7	853.7075	148.5631×10^{-6}
M13	3588.800	95.8142×10^{-6}

The information in table 8 were then used to obtained the values needed for the gain and bandwidth calculations as shown in Table 9 and 10.

Table 9:

Results for Amplifier's Total Output Resistance at 1V Operating Point for TSMC 250nm Technology

Quantity	Result
R_A	2.9711 KOhm
R_B	4.1978 KOhm
R_{nd}	6.6784 KOhm
R_{pd}	10.4066 KOhm
R	5.049.9250 KOhm
N	0.5667
R_{in1}	1.2195 MOhm
R_{in2}	4.34 MOhm
R_{out}	0.9522 MOhm

Table 10:

Results for Amplifier's Total Transconductance at 1 V Operating Point for TSMC 250nm Technology

Quantity	Result
R_A	2.9710 KOhm

R_B	17.0850 KOhm
R_C	17.0850 KOhm
R_D	4.1978 KOhm
R	0.5369 MOhm
C	3.44×10^{-9}
G_m	5.88×10^{-5}

From the previous two tables, it was obtained that the total amplifier gain is equal to

$$A = 2G_m R_{out} = 2\times 5.88\times 10^{-5}\times 0.9522\times 10^{6} = 111.956 V/V = 40.98 dB$$

As for the amplifier bandwidth, the quantities in table 4 can be used here as well because these are technology parameters. Using the information represented in table 4, the output capacitance and the bandwidth can be obtained to be equal to

$$C_{out} = C_D\big|_{NMOS} + C_D\big|_{PMOS} = 9.85\times 10^{-15} F$$

$$BW = 1/(2\pi R_{out} C_{out}) = 16.96\times 10^{6}\ Hz$$

To verify this information, the other two simulations were run. First to validate the value for the amplifier low frequency gain, time domain simulation is performed and the differential gain is measured to be equal to 41.4dB which lies within 1% error from the calculated value. Second, frequency domain simulation is performed to verify the gain, and bandwidth of the amplifier. The bandwidth at the 1V operating point is 18MHz. This result has an error around 6.5%. As discussed earlier, this large error due to

that fact that the bandwidth calculations are considered for the worst case condition.

1.5V Operating point with Small Output Devices

For this simulation setting, the 1.25V operating point is used but the output devices sizes were decreased. This is mainly to make sure that the formulation derived in the previous section can accommodate not only for supply change but also for different design values.

The same steps were done for the this simulation setup and the results are shown in the following tables

Table 11:

DC Operating Point Simulation at 1.5V operating point and small output devices for TSMC 250nm Technology

Device	R_o (KOhm)	g_m
M18	7.3549	Not Required
M19	7.3549	Not Required
M8	519.3237	337.7597×10^{-6}
M1	5.0105	Not Required
M2	5.0105	Not Required
M14	5239	164.8198×10^{-6}
M6	1405.3	84.5646×10^{-6}
M12	5652.4	54.332×10^{-6}
M7	1405.3	84.5646×10^{-6}

M13	5652.4	54.332×10^{-6}

The information in table 11 were then used to obtained the values needed for the gain and bandwidth calculations as shown in Table 12 and 13.

Table 12:

Results for Amplifier's Total Output Resistance at 1.5V Operating Point and Small Devices for TSMC 250nm Technology

Quantity	Result
R_A	2.5040 KOhm
R_B	3.6516 KOhm
R_{nd}	11.7266 KOhm
R_{pd}	18.3456 KOhm
R	5.1097 KOhm
N	0.5667
R_{in1}	1.7523 MOhm
R_{in2}	6.33MOhm
R_{out}	1.37 MOhm

Table 13:

Results for Amplifier's Total Transconductance at 1.5V Operating Point and Small Devices for TSMC 250nm Technology

Quantity	Result
R_A	2.5041 KOhm
R_B	30.0722 KOhm

R_C	30.072 KOhm
R_D	3.6516 KOhm
R	1.27 GOhm
C	1.29×10^{-9}
G_m	3.88×10^{-5}

From the previous two tables, it was obtained that the total amplifier gain is equal to

$$A = 2G_m R_{out} = 2 \times 3.88 \times 10^{-5} \times 1.37 \times 10^{6} = 106.62 V/V = 40.56 dB$$

As for the amplifier bandwidth, the quantities in table 4 can be used here as well because these are technology parameters. Using the information represented in table 4, the output capacitance and the bandwidth can be obtained to be equal to

$$C_{out} = C_D\big|_{NMOS} + C_D\big|_{PMOS} = 9.85 \times 10^{-15} F$$

$$BW = 1/(2\pi R_{out} C_{out}) = 11.79 \times 10^{6}\ Hz$$

To verify this information, the other two simulations were run. First to validate the value for the amplifier low frequency gain, time domain simulation is performed and the differential gain is measured to be equal to 40.97dB which lies within 1% error from the calculated value. Second, frequency domain simulation is performed to verify the gain, and bandwidth of the amplifier. The bandwidth at the 1.5V operating point with small output devices is 12.6MHz. This result has an error around 7%. As discussed earlier, this large error due to that fact that the bandwidth calculations are

considered for the worst case condition. Table 14 summarizes the aforementioned results.

Table 14:

Comparison Between Simulation and Analytical Results at Different Operating Points for TSMC 250nm Technology

Operating Conditions		Quantity		
		Output Resistance	Total Gain	BW
DC=1.5V Input=1mV	Calculated	0.909MOhm	40.26dB	17.78MHz
	Simulated	-	40.36dB	19MHz
	Error	-	0.25%	6.86%
		Output Resistance	Total Gain	BW
DC=1.25V Input=1mV	Calculated	0.959MOhm	41.29dB	16.85MHz
	Simulated	-	41.58	18MHZ
	Error	-	0.70%	6.39%
		Output Resistance	Total Gain	BW
DC=1.0V Input=1mV	Calculated	0.952MOhm	40.98dB	16.96MHZ
	Simulated	-	41.4dB	18MHz
	Error	-	1.02%	6.13%

TSMC 350nm Fabrication Technology

Mid-Rail Operating Point

The three aforementioned types of simulations were repeated for the TSMC 350nm Fabrication Technology. Table 15 shows the results of the DC operating point simulation at the mid-rail voltage operating point.

Table 15:

DC Operating Point Simulation at Mid rail operating point for TSMC 350nm Technology

Device	R_o (KOhm)	g_m
M18	10.2526	Not Required
M19	10.2526	Not Required
M8	1049.9	237.2622×10^{-6}
M1	8.0388	Not Required
M2	8.0388	Not Required
M14	862.1308	173.3434×10^{-6}
M6	1961.700	105.77×10^{-6}
M12	1159.900	89.9243×10^{-6}
M7	1961.700	105.77×10^{-6}
M13	1159.900	89.9243×10^{-6}

This information is then plugged into the aforementioned equations for the amplifier's total output resistance and total transconductance to obtain the results described in Table 16 and Table 17.

Table 16:

Results for Amplifier's Total Output Resistance at Mid-rail Operating Point for TSMC 350nm Technology

Quantity	Result
R_A	4.0007 KOhm
R_B	5.1014 KOhm
R_{nd}	9.4091 KOhm
R_{pd}	11.0149 KOhm
R	6.2962 KOhm
N	0.4175
R_{in1}	1546.1204 KOhm
R_{in2}	2509.7107 KOhm
R_{out}	956.7250 KOhm

Table 17:

Results for Amplifier's Total Transconductance at the Mid-rail operating Point for TSMC 350nm Technology

Quantity	Result
R_A	4.0007 KOhm
R_B	20.4240 KOhm
R_C	20.4240 KOhm
R_D	5.1014 KOhm
R	788.9434 MOhm
C	2.4132×10^{-9}
G_m	4.9287×10^{-5}

From the previous two tables, it was obtained that the total amplifier gain is equal to

$$A = 2G_m R_{out} = 2 \times 4.9287 \times 10^{-5} \times 0.9567 \times 10^{6} = 94.3081 V/V = 39.49 dB$$

As for the amplifier bandwidth, Table 18 shows the details needed to get the total output capacitance.

Table 18:

Device Characteristic Capacitances for TSMC 350nm Technology

Quantity	NMOS	PMOS
Junction Capacitance (C_J)	1.003925×10^{-3}	1.433541×10^{-3}
Side wall Capacitance (C_{JSW})	3.505428×10^{-10}	4.291576×10^{-10}
Gate Side wall Capacitance (C_{JSWG})	1.82×10^{-10}	4.42×10^{-10}
Diffusion Length (L_D)	2.9744×10^{-10}	0.0
C_D	2.66×10^{-15}	0

Using the information represented in table 18, the output capacitance and the bandwidth can be obtained to be equal to

$$C_{out} = C_D\big|_{NMOS} + C_D\big|_{PMOS} = 2.55 \times 10^{-15} F$$

$$BW = 1/(2\pi R_{out} C_{out}) = 62.43 \times 10^{6}\ Hz$$

To verify this information, the other two simulations were run. First to validate the value for the amplifier low frequency gain, time domain simulation is performed and the differential gain is measured to be equal to

39.82dB which lies within 1% error from the calculated value. Second, frequency domain simulation is performed to verify the gain, and bandwidth of the amplifier. The bandwidth at the 1.25V operating point with small output devices is 67.37MHz. This result has an error around 7%. As discussed earlier, this large error due to that fact that the bandwidth calculations are considered for the worst case condition.

TSMC 180nm Fabrication Technology

Mid-Rail Operating Point

The three aforementioned types of simulations were repeated for the TSMC 180nm Fabrication Technology. Table 19 shows the results of the DC operating point simulation at the mid-rail voltage operating point.

Table 19:

DC Operating Point Simulation at Mid rail operating point for TSMC 180nm Technology

Device	R_o (KOhm)	g_m
M18	6.0706	Not Required
M19	6.0706	Not Required
M8	366.5146	450.9513×10^{-6}
M1	4.0946	Not Required
M2	4.0946	Not Required
M14	630.7775	240.5597×10^{-6}
M6	733.3314	204.7059×10^{-6}
M12	1065.100	129.1086×10^{-6}

M7	733.3314	204.7059×10^{-6}
M13	1065.100	129.1086×10^{-6}

This information is then plugged into the aforementioned equations for the amplifier's total output resistance and total transconductance to obtain the results described in Table 20 and Table 21.

Table 20:

Results for Amplifier's Total Output Resistance at Mid-rail Operating Point for TSMC 180nm Technology

Quantity	Result
R_A	2.0407 KOhm
R_B	3.0104 KOhm
R_{nd}	4.8527 KOhm
R_{pd}	7.6895 KOhm
R	3.6009 KOhm
N	0.6802
R_{in1}	1103.484 KOhm
R_{in2}	1224.591 KOhm
R_{out}	580.4437 KOhm

Table 21:

Results for Amplifier's Total Transconductance at the Mid-rail operating Point for TSMC 180nm Technology

Quantity	Result
R_A	2.0407 KOhm

R_B	12.5422 KOhm
R_C	12.5422 KOhm
R_D	3.0104 KOhm
R	284.0103 MOhm
C	6.5083×10^{-9}
G_m	8.1629×10^{-5}

From the previous two tables, it was obtained that the total amplifier gain is equal to

$$A = 2G_m R_{out} = 2\times 8.1629\times10^{-5}\times 0.5804\times10^{6} = 94.761V/V = 39.53dB$$

As for the amplifier bandwidth, Table 22 shows the details needed to get the total output capacitance.

Table 22:

Device Characteristic Capacitances for TSMC 180nm Technology

Quantity	NMOS	PMOS
Junction Capacitance (C_J)	9.513993×10^{-4}	1.160855×10^{-3}
Side wall Capacitance (C_{JSW})	2.600853×10^{-10}	2.306564×10^{-10}
Gate Side wall Capacitance (C_{JSWG})	3.3×10^{-10}	4.22×10^{-10}
Diffusion Length (L_D)	1.7015×10^{-8}	2.7181×10^{-8}
C_D	3.04×10^{-15}	6.85

Using the information represented in table 22, the output capacitance and the bandwidth can be obtained to be equal to

$$C_{out} = C_D\big|_{NMOS} + C_D\big|_{PMOS} = 3.04\times10^{-15} + 6.85\times10^{-15} = 9.892.55\times10^{-15} F$$

$$BW=1/(2\pi R_{out}C_{out})=27.71\times10^{6}\ Hz$$

To verify this information, the other two simulations were run. First to validate the value for the amplifier low frequency gain, time domain simulation is performed and the differential gain is measured to be equal to 39.79dB which lies within 1% error from the calculated value. Second, frequency domain simulation is performed to verify the gain, and bandwidth of the amplifier. The bandwidth at the 1.25V operating point with small output devices is 29.75MHz. This result has an error around 7%. As discussed earlier, this large error due to that fact that the bandwidth calculations are considered for the worst case condition. Table 23 shows a summary of the results across the tested fabrication technologies

Table 23:

Comparison Between Simulation and Analytical Results at different process fabrication technologies

Operating Conditions		Quantity		
		Output Resistance	Total Gain	BW
TSMC 180nm DC=1.25V	Calculated	0.5804 MOhm	39.53dB	27.71 MHz
	Simulated	-	39.79dB	29.75 MHz
	Error	-	0.65%	6.85%
		Output Resistance	Total Gain	BW
TSMC 250nm DC=1.25V	Calculated	0.959MOhm	41.29dB	16.85MHz
	Simulated	-	41.58	18MHZ
	Error	-	0.70%	6.39%
		Output Resistance	Total Gain	BW
TSMC 350nm DC=1.25V	Calculated	0.9567 MOhm	39.49dB	62.43MHZ
	Simulated	-	39.82dB	67.37MHz
	Error	-	0.83%	7.3%

V. Results Discussion

In the previous sections, the importance of amplifier design was established. This was due to the versatility and wide spread usage of the operational amplifiers in several applications. Several basic topologies were introduced along with their advantages and disadvantages. However, many applications demand higher performance than that provided by these basic amplifiers. Consequently, several advanced topologies were introduced to further enhance the performance of such basic amplifiers. The advanced operational amplifiers offered a sufficient solution to many applications but in the same time, other design issues emerged that made the design problem much more complicated. These design issues include process variability tolerance, biasing issues, and complexity of the amplifier design equations. Several attempts were made to come up with an efficient amplifier topology that minimizes the effects of these issues. The fully differential self biased folded cascode amplifier was introduced as an instance of the family of self biased fully differential amplifiers. This amplifier topology was characterized to make sure that its design properties fit the criteria needed to counteract the described design problems. Several quantities were obtained to establish the usefulness and superiority of such topology. These quantities included the amplifier CMRR, PSRR, CMR, temperature drift, and input and output impedances. This fully differential self biased folded cascode amplifier possesses a unique feature of being self biased. The amplifier uses the replica chains self biasing technique introduced by Abdelmoneum et al. [25]. This technique simply replicates the output devices and uses these replicated devices to bias the internal amplifier points. This self bias

technique helps solve several design problems such as external supply voltage variations and manufacturing process variability. First, external supply poses the issue of supply noise and the need for larger packages to accommodate for the input pins. Also, the process variations always pose a challenge during the design process because the bias point needs to change in accordance with the process variations. The replica chains biasing technique eliminated these problems. Being an internal point in the amplifier, the need for external power supplies is eliminated. In addition, the internal bias point changes with process variations like any other internal node in the amplifier thus making the self bias point adapts to the process variation. To prove the usefulness of this amplifier, it was used to design an oscillator circuit for MEMS devices as described in [26]. This application tested the self bias feature of the amplifier because the oscillator design mandates that the amplifier changes its gain and, in turn, its operating point. Hence, a conventional external biasing solution would have been very tedious.

After proving its usefulness, the fully differential self biased folded cascode amplifier is used to test the technique of obtaining the design equations for the family of the complementary differential amplifiers. The amplifier gain and bandwidth were analyzed and detailed design equations for the total amplifier resistance, total amplifier transconductance, and total amplifier output capacitance were obtained. These design equations were then simplified and special cases were discussed. In the previous section, the results of applying the design equation to a realization of the described amplifier were compared to simulated data across different operating points, devices sizes and fabrication processes. The design equations were proved to

be accurate to within 1% error for the gain and within 7% for the bandwidth. The reason for the relatively high error percentage for the bandwidth is that the equation for the overall output capacitance did not include the effect of inverse bias on the device junctions. Thus, the resulting equation will always describe the worst case capacitance and hence the calculated bandwidth will be always lower than its simulated value. This inaccuracy cannot be considered a critical issue because the resulting bandwidth will be always lower than the actual bandwidth. Hence, if the design equations can meet the specifications on bandwidth, the actual bandwidth will be slightly higher and the design specification will still be met.

Being proved accurate, the obtained formulations can be utilized in many applications. First, during initial design phases, circuit designers usually require relatively simple and efficient design equations for the circuit under investigation. This enables them to predict how the design will perform under certain operating conditions. Consequently, the described derivation technique enables the designer to quickly derive the design equations for any complementary fully differential amplifier. Also, this work gives detailed application of such derivation technique on the fully differential self biased folded cascode amplifier. Hence, if needed, these equations can be directly used to design folded cascode amplifiers easily and accurately. In addition, several simplifications and special cases were analyzed thus enabling the designers to use the simplified equations to quickly gain insight about their amplifier design, whether it can achieve the design requirements or not, before getting into more detailed analysis of the design.

Second, this technique can be incorporated into software design kits in order to facilitate amplifier design process. This is because this work has proposed a general technique to obtain the design equations for the family of differential complementary amplifiers. Consequently, the designer may only need to draw the amplifier schematic, and input it to a software simulator then the software will be able to analyze the topology and return the design equations that the designer can directly use to gain insight into his/her design. Also, in case of designing fully differential self biased folded cascode amplifiers, the software can directly use the equations derived here to simulate the performance of the amplifier without going into more complex or more lengthy calculations.

VI. Conclusion

In the previous discussions, some Op-Amp architectures and a few techniques to eliminate the problem of biasing were introduced. This research focused on the family of fully differential complementary amplifiers to derive the equations for the amplifiers gain and bandwidth. The folded cascode fully differential amplifier was introduced as an instance of this family. Its self biasing technique, replica chains, was introduced and the amplifier was characterized to prove its usefulness. Then, it was used in an oscillator design to prove that the replica chain biasing technique is capable of adapting to the change in the amplifier operating point. A new mathematical model, which is based on the outlined derivation technique, for the folded cascode amplifier was introduced to calculate the Op-Amp parameters such as voltage gain, and operating bandwidth using information about the amplifiers' total output resistance, total transconductance, and total output capacitance. These models were then verified using circuit simulations and verified to be within acceptable error percentages.

Furthermore, several special case simplifications were introduced to facilitate handling the model if the conditions for the simplifications are met in a certain design. The outlined derivation can become a very important tool for circuit designers to help them achieve their design goals efficiently without wasting time in trial and error phase. Also, this derivation can be incorporated to a circuits software design kit to help the designers characterize the designed any full differential complementary amplifier in general or fully differential self biased folded cascode in specific.

One recommendation to further develop the mathematical model is to include the effects of short channel effects in the derivations. This is because the derivation proved accurate for devices with relatively large sizes as their models are well understood, documented, and incorporated in most of the circuit simulators. However, as fabrication technology becomes smaller and smaller, these above formulations can be used as a guideline or an initial design step that provides an approximation for the circuit behavior which will minimize the time required for designing the amplifier compared to trial and error techniques that are used at the moment. Thus, such short channel derivation expansion can be very useful to both researchers and designers.

In the end, these mathematical formulations, besides their corresponding amplifier topology, are proved to be very helpful to analog circuit designers whenever a stable self-biased amplifier is needed.

VII. Appendices

A. Appendix A: Model Simplifications and Special Cases

In the aforementioned discussion, a hyppthetical special case of interest was considered. It was the case of the symmetric complementary circuit. These set of characteristics can represented by the following set of equations

$$r_{o,M6} = r_{o,M7} = r_{o,M12} = r_{o,M13} = r_o \qquad \text{(A1)}$$

$$g_{m,M6} = g_{m,M7} = g_{m,M12} = g_{m,M13} = g_m \qquad \text{(A2)}$$

$$\mu_p W_p = \mu_n W_n \qquad \text{(A3)}$$

Equation A1 simply states that the NMOS devices in the output stage have the same output resistance as well as the PMOS devices. Furthermore, it states that both NMOS and PMOS devices have the same output resistance due to the complementary nature of the design. Equation A2 states the same but for the device transconductance. In addition, equation A3 mandates that both NMOS and PMOS devices have the same current driving strengths. Applying these conditions to the amplifier output resistance equations will result in the following equations.

$$R_B = R_A = \frac{r_o}{2} \qquad \text{(A4)}$$

$$R_{pd} = R_{nd} = \frac{1}{g_m} \tag{A5}$$

$$R = (R_{pd} + R_{nd}) || (R_A + R_B) = \left(\frac{2}{g_m} \right) || r_o \tag{A6}$$

$$= \frac{2r_0}{2 + g_m r_o}$$

$$N = \frac{\mu_p W_p}{\mu_n W_n + \mu_p W_p} = \frac{1}{2} \tag{A7}$$

$$R_{in1} = R_{in2} = R_{in} = \left[\frac{g_m R}{2} + 1 \right] r_o \tag{A8}$$

$$= \left[\frac{2 + 2 r_o g_m}{2 + r_o g_m} \right] r_o$$

$$R_{out} = \frac{R_{in}}{2} = \left[\frac{1 + r_o g_m}{2 + r_o g_m} \right] r_o \tag{A9}$$

Equation A9 presents the end results of the series of simplifications. As was noted, this means that for high values of device transconductance, the total output resistance will only depend on the device output resistance itself in the case of full complementary and symmetric design.

As for the total amplifier transconductance, Equation A10 presents the simplification results due to the complementary design. It states that both PMOS and NMOS devices are having the same current driving capabilities and thus having the same device transconductance

$$g_{m,M8} = g_{m,M14} \tag{A10}$$

$$R_B = R_C = \left(\frac{2}{g_m}\right) \tag{A11}$$

$$R_A = R_D = \frac{r_o}{2} \tag{A12}$$

$$\begin{aligned} R &= (R_B + R_C)(R_A + R_D + R_B||R_C) \\ &= \left(\frac{4}{g_m}\right)\left(r_o + \frac{1}{g_m}\right) = \frac{4}{g_m^2}(1 + r_o g_m) \end{aligned} \tag{A13}$$

$$\begin{aligned} C &= \frac{R_A g_{m,M14}}{R} + \frac{R_D g_{m,M8}}{R} \\ &= \frac{r_o g_m^3}{4(1 + r_o g_m)} \end{aligned} \tag{A14}$$

$$G_m = CR_B = \frac{r_o g_m^2}{2(1 + r_o g_m)} \tag{A15}$$

Equation A10 can then be followed by the series of simplifications outlined by Equations A11 through Equation A15. Therefore, the overall gain can finally be represented by Equation A16

$$\begin{aligned} A &= 2G_m R_{out} = \frac{r_o g_m^2}{2(1 + r_o g_m)}\left[\frac{1 + r_o g_m}{2 + r_o g_m}\right] r_o \\ &= \frac{(r_o g_m)^2}{(2 + r_o g_m)} \end{aligned} \tag{A16}$$

B. Appendix B: Transistor Sizing tables

Figure B1 shows the amplifier topology used during this work.

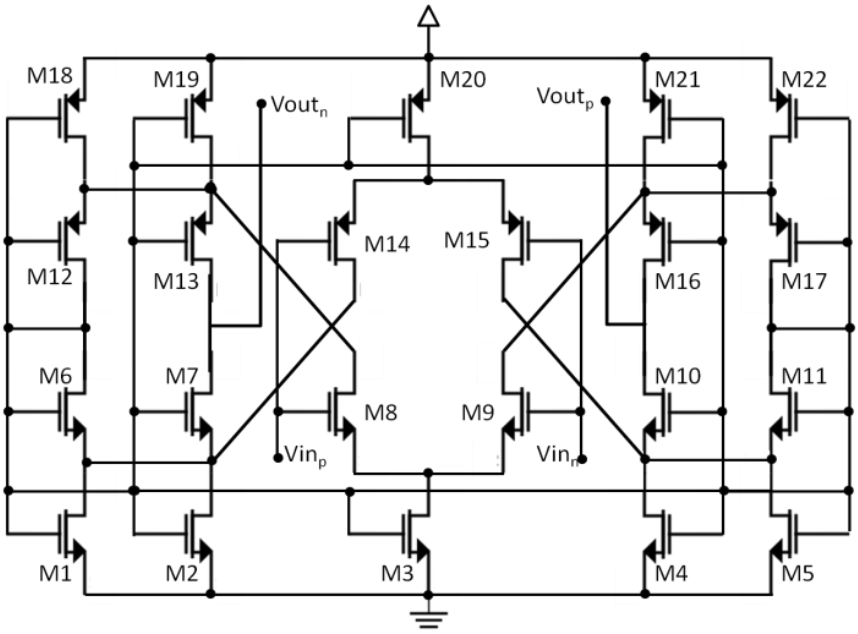

Figure B1: Folded Cascode Amplifier Revisited

Normal Device Sizes

Table B1

Device Sizes for the Normal Operation

Device	Size (W/L)
M1	2.5
M2	2.5
M3	5
M4	2.5
M5	2.5
M6	2.5
M7	2.5
M8	5
M9	5
M10	2.5
M11	2.5
M12	5
M13	5

M14	10
M15	10
M16	5
M17	5
M18	5
M19	5
M20	10
M21	5
M22	5

Small Device Sizes

Table B1

Device Sizes for the Normal Operation

Device	Size (W/L)
M1	2.5
M2	2.5
M3	5
M4	2.5
M5	2.5
M6	1.25
M7	1.25
M8	5
M9	5
M10	1.25
M11	1.25
M12	2.5
M13	2.5
M14	10
M15	10
M16	2.5
M17	2.5
M18	5
M19	5
M20	10
M21	5
M22	5

VIII. References

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