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Design of the fully differential operational floating conveyor and its applications

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DESIGN OF THE FULLY DIFFERENTIAL OPERATIONAL FLOATING CONVEYOR (FD-OFC) AND ITS APPLICATIONS

A Thesis Submitted to

Electronics and Communications Engineering Department

in partial fulfillment of the requirements for

the degree of Master of Science

by Hossam ElGemmazy

under the supervision of

Prof. Yehea Ismail

Dr. Amr Helmy

Dr. Hassan Mostafa

September / 2017

The American University in Cairo

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Affiliation _____

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Dept. Chair/Director	**Date**	**Dean**	**Date**

DEDICATION

To my parents and my wife for their endless love, support and encouragement

ACKNOWLEDGMENTS

First of all, I would like to thank God for providing me with persistence and patience to complete this work.

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ABSTRACT

The American University in Cairo
Electronics and Communications Engineering Department
"Design of the Fully Differential Operational Floating Conveyor (FD-OFC) and its Applications"
Name: Hossam ElGemmazy
Thesis Supervisors: Prof. Yehea Ismail, Dr. Amr Helmy, Dr. Hassan Mostafa

Analog circuits can be generally classified into two broad categories: The first one includes analog circuits operating in the voltage mode, while the second category includes those operating in the current mode. Voltage mode analog circuit's bandwidth is highly dependent on the gain via the gain bandwidth product (GBP). To solve this problem, many current mode circuits are developed such as the second generation Current Conveyor (CCII) and the Operational Floating Conveyor (OFC).

A novel concept of the Fully Differential Operational Floating Conveyor (FD-OFC) is presented for the first time, to the best of the author's knowledge. A CMOS design for the proposed FD-OFC is introduced as an 8 (4x4) port general purpose analog building block. The FD-OFC design is implemented using two different realizations. The proposed design has the advantage of low power consumption as it operates under biasing conditions of only 1.2 V while its wide bandwidth reaches 600 MHz. These operating conditions recommend the proposed device to be integrated to a wide range of low power-wide high speed applications. The terminal behavior of the proposed device is mathematically modeled and its operation is simulated using the UMC 130 nm technology kit in Cadence environment.

Differential voltage amplifier, current mode instrumentation amplifier (CMIA) and Fully Differential second generation Current Conveyor (FDCCII) are examples of the presented applications based on the proposed FD-OFC.

Table of Contents

List of Figures

List of Tables

List of Abbreviations

DC	Direct Current
AC	Alternating Current
BJT	Bipolar Junction Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CMOS	Complementary Metal Oxide Semiconductor
VCVS	Voltage Controlled Voltage Source
CCVS	Current Controlled Voltage Source
VCCS	Voltage Controlled Current Source
CCCS	Current Controlled Current Source
VFOA	Voltage Feedback Operational Amplifier
CFOA	Current Feedback Operational Amplifier
BW	Bandwidth
GBP	Gain Bandwidth Product
VLSI	Very Large Scale Integrated circuits
CCI	First generation Current Conveyor
CCII	Second generation Current Conveyor
CCII+	Positive/Non-inverting second generation Current Conveyor
CCII-	Negative/Inverting second generation Current Conveyor
CCCII	Second generation Current Controlled Conveyor
CCIII	Third generation Current Conveyor
FDCCII+	Fully Differential Non-inverting second generation current conveyor
FDCCII-	Fully Differential Inverting second generation current conveyor
OFC	Operational Floating Conveyor
OFCC	Operational Floating Current Conveyor
FD-OFC	Fully Differential Operational Floating Conveyor
Zt	Trans-impedance gain
CMIA	Current Mode Instrumentation Amplifier
CMRR	Common Mode Rejection Ratio
dB	Decibel

Chapter 1: Introduction

1.1 Analog circuits

Analog circuits are essentially required in many fields since all natural signals are analog. Despite the dominance of digital circuits and techniques, analog circuits and techniques are still fundamental in many applications like signal amplifiers, sinusoidal oscillators, analog-to-digital converters and digital-to-analog converters. Even if many researchers have predicted a reduced utilization of analog architectures, analog circuits continue to be necessary.

Active analog circuits usually rely on various configurations based on operational amplifier (Op-Amp). These configurations operate either in the voltage mode (where voltage is the active parameter) or in the current mode (where current is the active parameter). Generally, analog circuits can be classified into voltage mode category and current mode category. Although the voltage mode circuits are employed in many analog signal processing applications, these circuits possess a fixed gain bandwidth product (GBP). The fixed GBP means that the bandwidth is highly dependent on the gain which induces a trade-off between these two quantities. Commonly, the trade-off is tailored to each particular application. This limitation has been overcome by adopting the current as the active parameter instead of the voltage. This concept has led to the development of many current mode based devices.

1.2 Current mode devices

The current mode based devices provide a degenerate gain bandwidth relationship where the GBP is not constant. Having a large bandwidth while preserving a high gain is the most important advantage offered by these current mode based devices. Moreover, current mode based devices provide larger dynamic range and higher slew rate compared to their voltage mode based counterparts. Due to these and other advantages, the research interests have been directed to the development of

such devices as they are perfect candidates for wide range of analog applications such as biomedical instrumentation and data acquisition devices.

The first generation Current Conveyor (CCI) has been introduced by Sedra and Smith in 1968 [8] as the first current mode device. Sedra and Smith also introduced the second generation Current Conveyor (CCII) in 1970 [9]. Since then, several current mode based devices have been developed [2,10] along with their applications. The Fully Differential Current Conveyor (FDCCII) is introduced as the fully differential form of the current conveyor.

The Operational Floating Conveyor (OFC) [23] and the Operational Floating Current Conveyor (OFCC) [28] are examples of the developed devices that offer more features than the CCII. The novel concept of the Fully Differential Operational Floating Conveyor (FD-OFC) is proposed in this thesis as the fully differential form of the OFC. The FD-OFC is a general purpose building block for analog VLSI applications.

1.3 Organization of the thesis

The rest of the thesis is organized as follows:

Chapter 2 contains an overview of different current mode devices along with their mathematical model through historical development approach. The differences between current mode and voltage mode devices are highlighted. The principle operation of each device is reviewed and the terminal behavior is characterized.

Chapter 3 introduces the newly developed concept of the Fully Differential Operational Floating Conveyor (FD-OFC) and its CMOS-based designs. The proposed FD-OFC terminal behavior is presented and its performance is investigated via simulation results.

Chapter 4 presents different applications based on FD-OFC such as fully differential voltage amplifier, fully differential integrator and current mode instrumentation amplifier (CMIA). The performance of each application is verified through simulation results.

Finally, Chapter 5 provides the thesis conclusion and states the suggested future work.

Chapter 2: Background and Literature Review

2.1 Introduction

This chapter contains the background and brief literature review of the main types of current mode devices. The advantages of current mode devices compared to voltage mode devices are explained. The operation of each device is reviewed along with its mathematical model and terminal behavior. First generation Current Conveyor (CCI), second generation Current Conveyor (CCII), Operational Floating Conveyor (OFC) and Operational Floating Current Conveyor (OFCC) are examples of current mode devices. Different implementations of these devices are presented.

2.2 Current mode versus voltage mode

Analog circuits can be generally classifies into two broad categories. The first category includes analog circuits operating in the voltage mode where the voltage is the active parameter. The second category includes analog circuits operating in the current mode where the current is the active parameter. The voltage mode analog circuits are used to be more popular and employed in many analog signal processing applications. In the past two decades, the current mode circuits have emerged as an important category of analog circuits due to the following advantages:

Firstly, current mode circuits offer higher frequency capabilities than the corresponding voltage mode circuits. The current mode devices exhibit larger bandwidth while preserving high gain. This feature is achieved because the gain bandwidth product (GBP) is not fixed for the current mode devices. On the other hand, the voltage mode devices suffer from fixed GBP which means that the bandwidth is highly dependent on the gain (trade-off).

Secondly, the supply voltage is forced to scale down due to the continuous scaling in the technology feature size. This continuous reduction in supply voltage prevents the breakdown of devices but it limits the dynamic range of the voltage

signals. On the other hand, for the current mode circuits the supply voltage reduction doesn't limit the current level flowing between nodes. This means higher dynamic range compared to the voltage mode circuits.

Other advantages of current mode circuits include better accuracy, better linearity and higher slew rate compared to voltage mode counterparts [1,2]. All these advantages are the motive that directed analog designers and researcher to represent the signal as current instead of voltage. This interest has led to spending more time and effort in exploring and developing different current mode devices.

2.3 History of current conveyors

The Current Conveyors were invented by Sedra and Smith in the late sixties and early seventies. They introduced the first generation Current Conveyor (CCI) in 1968 [8]. Figure 2-1 depicts a simplified block diagram representation of the first generation current conveyor CCI.

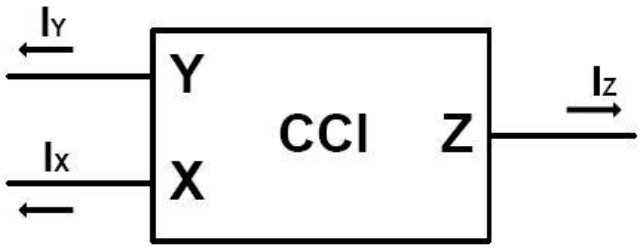


Figure 2-1: Block diagram representation of CCI

The CCI is a three terminal device where X and Y are the input terminals while Z is the output terminal. The principle of operation of the CCI can be briefly summarized as follows: The voltage applied at terminal Y exactly appears at terminal X which represents the voltage following action at input terminals (X and Y). The forced current at terminal X exactly flows at terminal Y. The voltage at terminal X is independent on the forced current I_X at the same terminal. Similarly, the flowing current at terminal Y (I_Y) is independent on the voltage at the same terminal. The input impedance of X and Y terminals are ideally zero. The current following action

is accomplished by conveying the current I_X to the output terminal Z. the output impedance of terminal Z is ideally infinite. So, terminal Z has the same characteristics of current source. This mechanism of operation can be represented using the following matrix notation as:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (2\text{-}1)$$

Figure 2-2 shows the first circuit design of the current conveyor CCI based on the Bipolar Junction Transistors (BJT) technology [8].

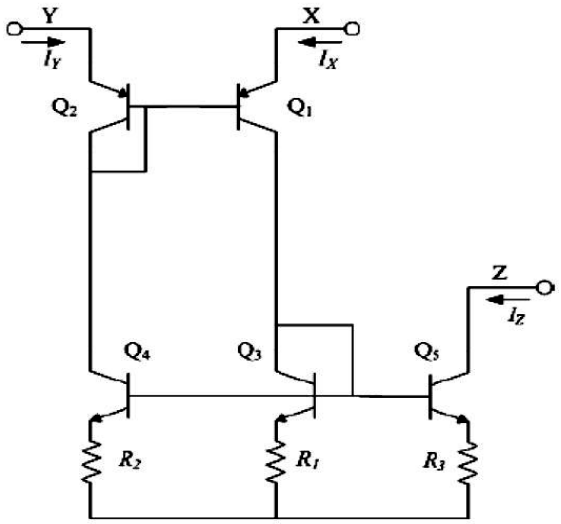


Figure 2-2: The first implementation of CCI using BJT [8]

In 1970 Sedra and Smith came up with the second generation Current Conveyor (CCII) which is more versatile version of the CCI [9]. Figure 2-3 depicts a simplified block diagram representation for the inverting and non-inverting versions of the second generation current conveyor CCII+/-. Figure 2-4 shows one of the CMOS implementations of CCII+ [12].

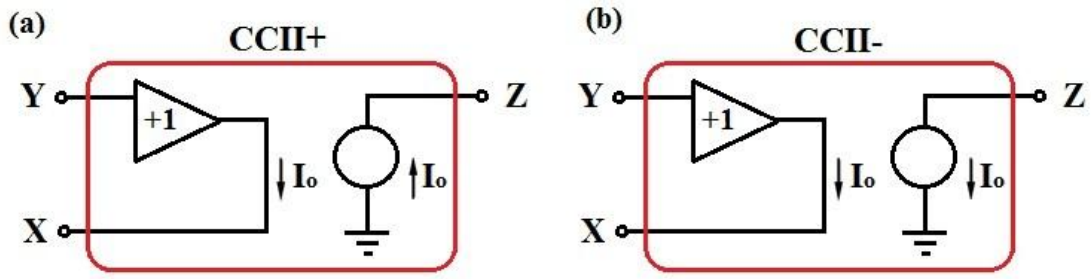


Figure 2-3: Block diagram representation of (a) CCII+ (b) CCII-

The principle of operation of the CCII can be briefly summarized as follows: The voltage applied at terminal Y exactly appears at terminal X which represents the voltage following action at input terminals (X and Y). The current at terminal Y equals zero due to the infinite input impedance of terminal Y. The voltage at terminal X is independent on the forced current I_O at the same terminal. The input impedance of terminal X is ideally zero. The current following action is accomplished by conveying the current I_O to the output terminal Z. the output impedance of terminal Z is ideally infinite. So, terminal Z has the same characteristics of current source. The current at terminal Z can be in-phase or out of phase with terminal X current I_O based on the current conveyor version (CCII+ or CCII-). For CCII+, the currents of X and Z terminals are flowing in the same direction. For CCII-, the currents of X and Z terminals are flowing in opposite directions. This mechanism of operation can be represented using the following matrix notation as:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \qquad (2\text{-}2)$$

(where the + and – signs correspond to the CCII+ and the CCII- respectively)

The main high performance measures of the CCII are: high accuracy in voltage and current transfer, wide input voltage and current ranges, low input impedance at terminal X, high output impedance at terminal Z and wide bandwidth for voltage and current transfer.

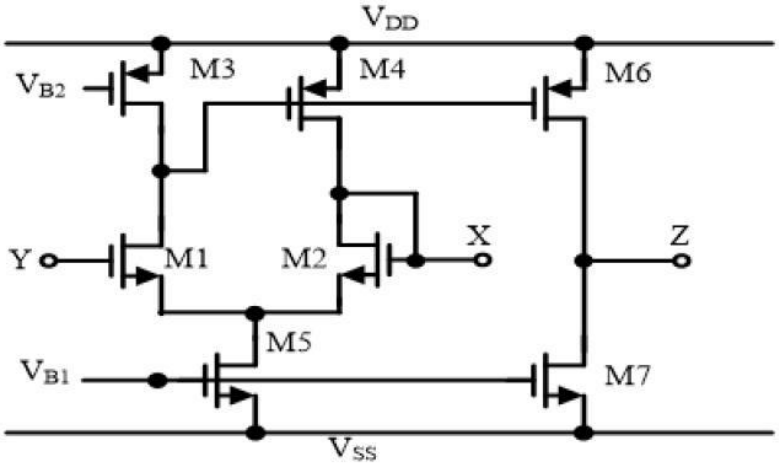


Figure 2-4: CMOS implementation of CCII+ [12]

A third generation of the Current Conveyor CCIII was introduced later by Fabre in 1995 [11]. The operation of the CCIII is similar to the operation of CCI except for only one difference. This difference is that the flowing current in terminal Y is in the opposite direction of the flowing current in terminal X. This mechanism of operation can be represented using the following matrix notation as:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (2\text{-}3)$$

2.4 Fully Differential Current Conveyor (FDCCII)

The Fully Differential second generation Current Conveyor (FDCCII) was proposed by El-Adawy, Soliman and Elwan in 2000 [16]. As its name implies, the FDCCII is the fully differential form of the CCII. El-Adawy et al. presented a CMOS implementation of the FDCCII+ as shown in Figure 2-5 and suggested many applications. The FDCCII as a fully differential device has the advantages of larger dynamic range, higher design flexibility (from the integration point of view) and higher noise rejection capabilities.

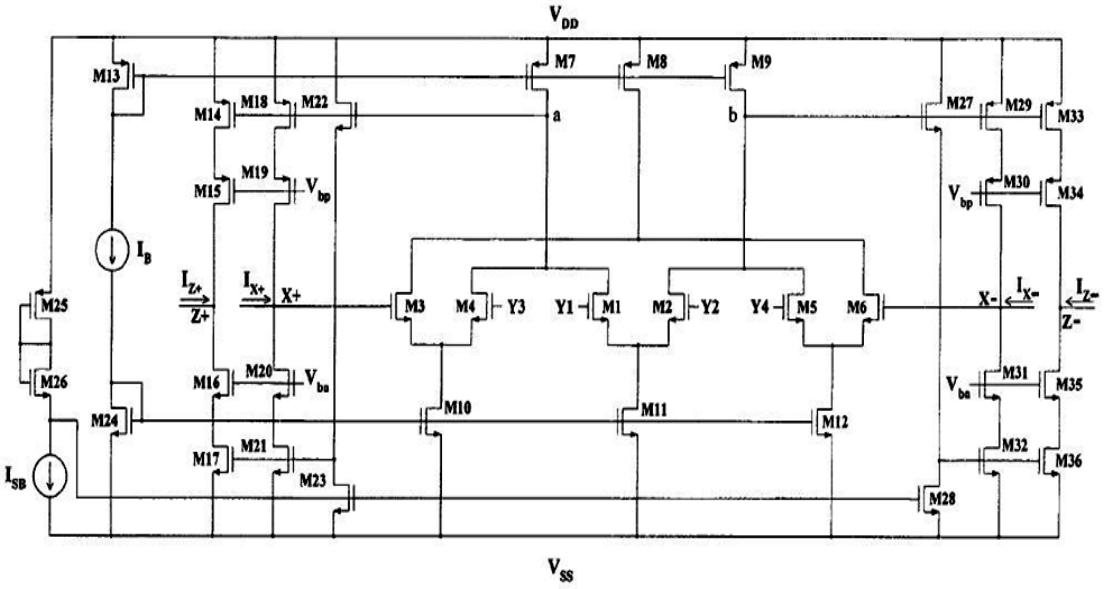


Figure 2-5: CMOS realization of the FDCCII+ [16]

Generally, the FDCCII can be represented as a six terminal device. The differential action is achieved by splitting each of the three terminals of the CCII into two terminals as shown in Figure 2-6. Both inverting and non-inverting versions of the FDCCII exist (FDCCII+ and FDCCII-).

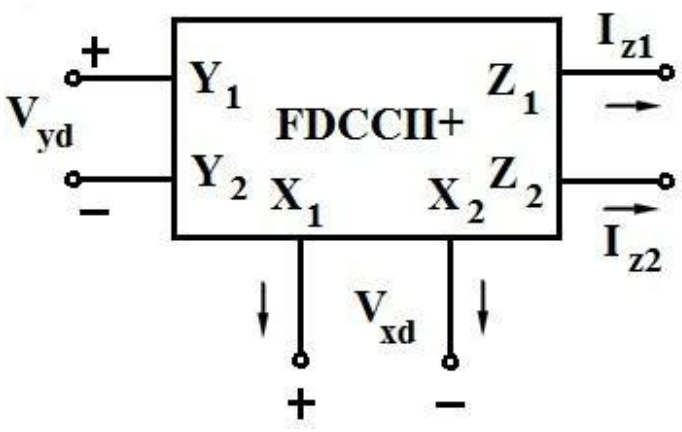


Figure 2-6: Block diagram representation of the FDCCII

The principle of operation of the FDCCII can be explained as follows: The differential input voltage applied at terminal Y ($V_{yd} = V_{y1} - V_{y2}$) ideally appears as a differential voltage at terminal X ($V_{xd} = V_{x1} - V_{x2}$) regardless of the forced current at

this terminal. This is the same voltage following action at the input ports as in the CCII. The input impedance of terminal X is ideally zero. The currents at the individual terminals Y_1 and Y_2 are zero due to the infinite input impedance of terminal Y. The currents I_{x1} and I_{x2} are conveyed to the output differential terminals Z as $I_{z1} = I_{x1}$ and $I_{z2} = I_{x2}$, respectively. The output impedance of terminal Z is ideally infinite. The input-output terminal behavior can be expressed by the transfer matrix of the FDCCII+/- "$T^{(FDCCII+/-)}$" as follows:

$$\begin{bmatrix} I_{yd} \\ V_{xd} \\ I_{zd} \end{bmatrix} = T^{(FDCCII+/-)} \begin{bmatrix} V_{yd} \\ I_{xd} \\ V_{zd} \end{bmatrix} \tag{2-4}$$

The (i ,j) entry of the FDCCII+/- transfer matrix "$T^{(FDCCII+/-)}$" is given by:

$$\left(T^{(FDCCII+/-)}\right)_{ij} = I_2 \otimes \left(T^{(CCII+/-)}\right)_{ij} \tag{2-5}$$

Where, I_2 is the a 2x2 identity matrix, $T^{(CCII+/-)}$ is the transfer matrix of the CCII+/- and $\otimes$ is the Kronicker product.

$$I_2 = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \tag{2-6}$$

$$T^{(FDCCII+/-)} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \tag{2-7}$$

$$\begin{aligned} I_{xd} &= \begin{bmatrix} I_{x1} & I_{x2} \end{bmatrix}^T, \quad I_{yd} = \begin{bmatrix} I_{y1} & I_{y2} \end{bmatrix}^T, \quad I_{zd} = \begin{bmatrix} I_{z1} & I_{z2} \end{bmatrix}^T, \\ V_{xd} &= \begin{bmatrix} V_{x1} & V_{x2} \end{bmatrix}^T, \quad V_{yd} = \begin{bmatrix} V_{y1} & V_{y2} \end{bmatrix}^T, \quad V_{zd} = \begin{bmatrix} V_{z1} & V_{z2} \end{bmatrix}^T \end{aligned} \tag{2-8}$$

And $[.]^T$ denotes the matrix transpose operator.

Accordingly, the FDCCII+/- transfer matrix can be expanded as follows:

$$T^{(FDCCII+/-)} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & \pm 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & \pm 1 & 0 & 0 \end{bmatrix} \tag{2-9}$$

$$\begin{bmatrix} I_{y1} \\ I_{y2} \\ V_{x1} \\ V_{x2} \\ I_{z1} \\ I_{z2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & \pm 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & \pm 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{y1} \\ V_{y2} \\ I_{x1} \\ I_{x2} \\ V_{z1} \\ V_{z2} \end{bmatrix} \tag{2-10}$$

(where the + and – signs correspond to the FDCCII+ and the FDCCII- respectively)

The FDCCII is the main building block for the designs proposed in this thesis. Different CMOS realization of the FDCCII and applications are introduced during the past years [16-22]. Figure 2-7 displays another FDCCII+ implementation while Figures 2-8 and 2-9 display two different implementations for the FDCCII-. A comparison between different FDCCII structures is presented in chapter 3.

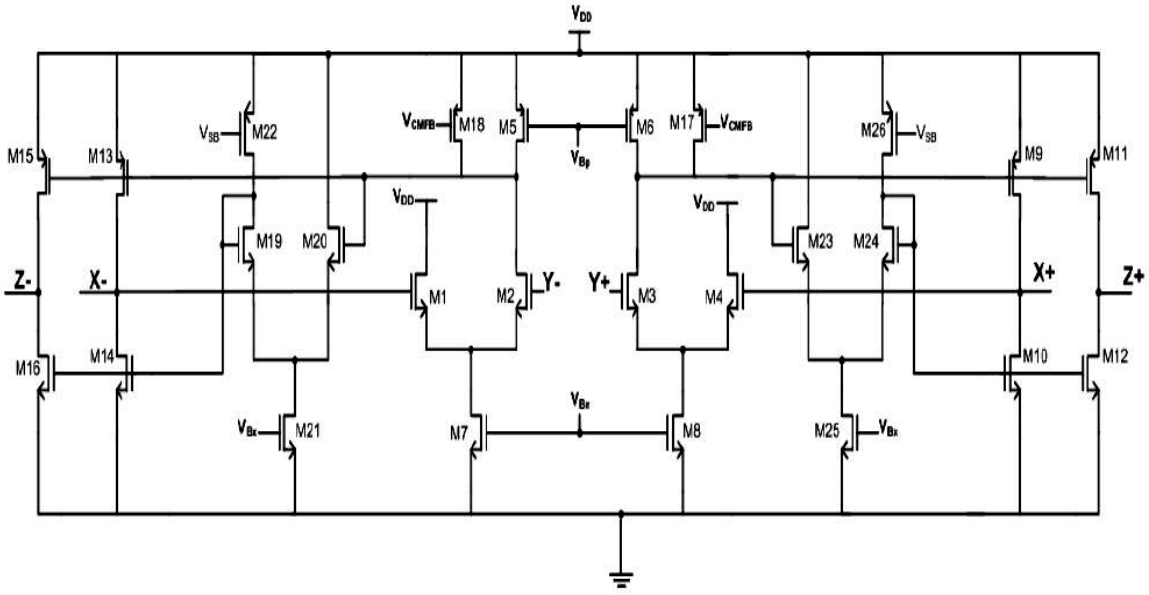


Figure 2-7: CMOS realization of the FDCCII+ [18]

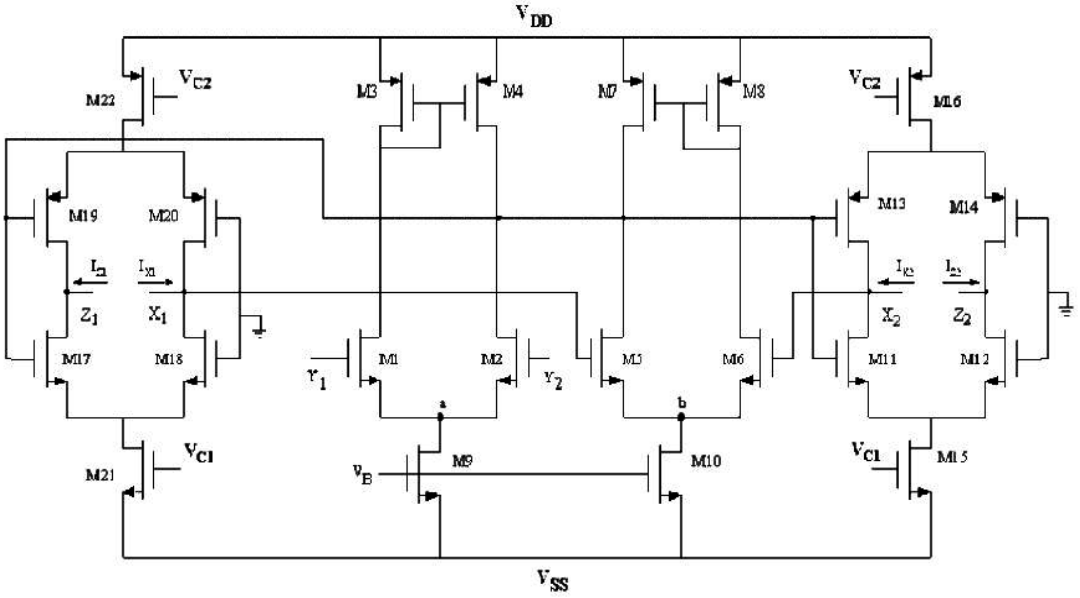


Figure 2-8: CMOS realization of the FDCCII- [19]

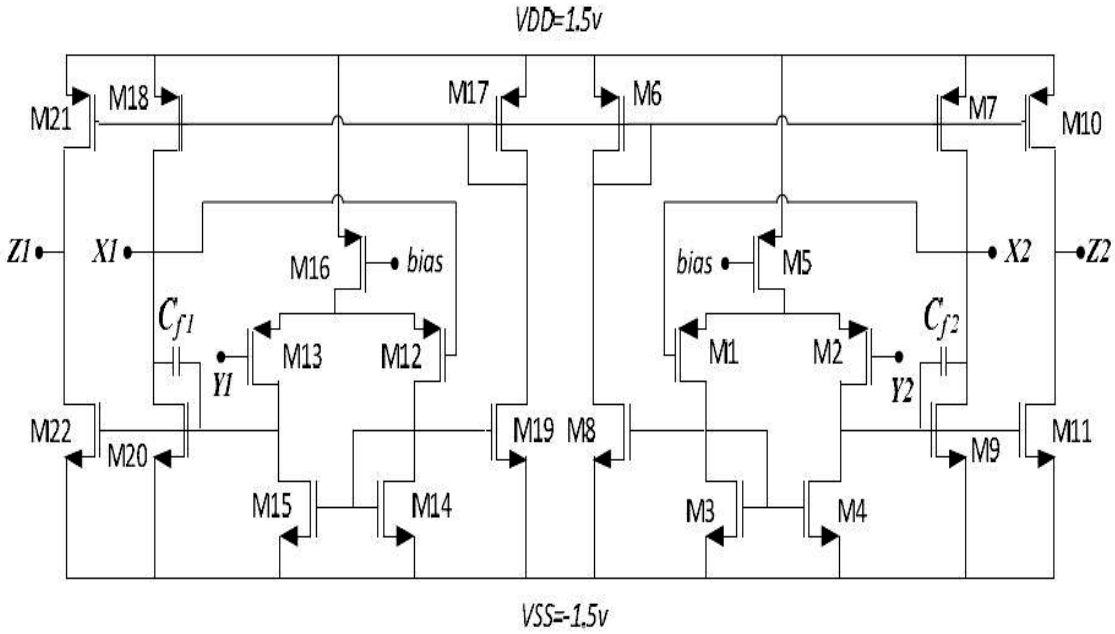


Figure 2-9: CMOS realization of the FDCCII- [21,22]

2.5 Current Feedback Operational Amplifier (CFOA)

The CFOA was introduced by Nelson and Evans in 1985 as a new approach to Op-Amp design [3]. The CFOA block diagram can be illustrated in Figure 2-10. The design of CFOA as a three terminal device is based on using CCII+ followed by a buffer where the CFOA trans-impedance is represented by Zt [5]. CFOA can be used to implement many applications like active filters, integrators and oscillators [4].

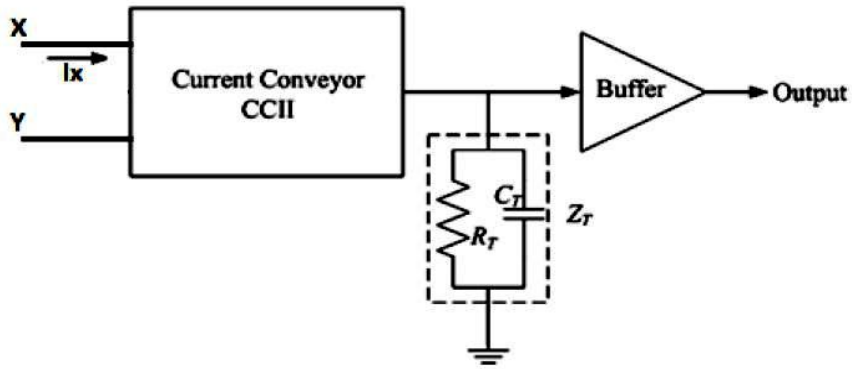


Figure 2-10: CFOA block diagram [5]

The operation of the CFOA can be briefly summarized as follows: Terminal Y is the CFOA non-inverting terminal while terminal X is the inverting terminal. The voltage applied at terminal Y exactly appears at terminal X which represents the voltage following action at input terminals (X and Y). This voltage following action is achieved using the CCII+. The current at terminal Y equals zero due to the infinite input impedance of terminal Y. The voltage at terminal X is independent on the forced current I_X at the same terminal. The input impedance of terminal X is ideally zero. The input current at terminal X is multiplied by the open loop trans-impedance gain Zt to produce a voltage at the buffer input. This voltage is transferred to the output terminal through the buffer. The output terminal impedance is ideally zero. This mechanism of operation can be represented using the following matrix form as:

$$\begin{bmatrix} I_Y \\ V_X \\ V_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & Zt & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ I_O \end{bmatrix} \qquad (2\text{-}11)$$

2.5.1 Voltage versus Current Feedback Operational Amplifiers

The ideal models for both Voltage Feedback Operational Amplifier (VFOA) and Current Feedback Operational Amplifier (CFOA) are displayed in Figures 2-11 and 2-12 respectively. The VFOA (conventional Op-Amp) is a voltage mode device while the CFOA (also known as trans-impedance Op-Amp) is a current mode device [6-7].

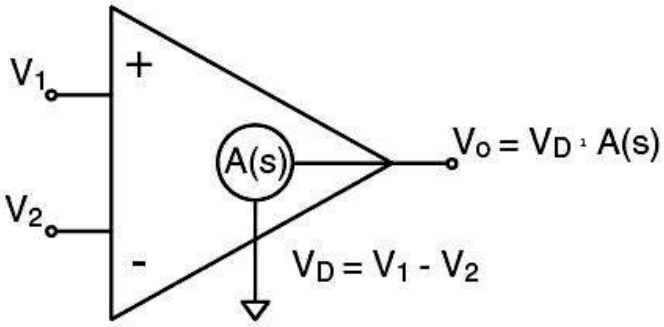


Figure 2-11: VFOA ideal model [7]

For the VFOA, the input impedance of both inverting and non-inverting terminals equals infinity. The output impedance equals zero. The output voltage equals the open loop voltage gain A(s) multiplied by the voltage difference between the input terminals (V_1-V_2).

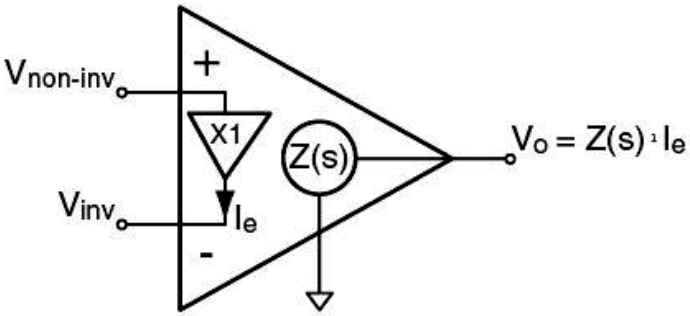


Figure 2-12: CFOA ideal model [7]

For the CFOA, the input impedance of the non-inverting terminal equals infinity while the input impedance of the inverting terminal equals zero. The output impedance equals zero. The output voltage equals the open loop trans-impedance gain Zt(s) multiplied by the input current.

The main advantages for the CFOA compared to VFOA are: It provides larger output current capability. The CFOA has higher slew rate which gives higher full power bandwidth. The CFOA exhibits gain-feedback independency which provides higher bandwidth for high gain. This can be explained using Figure 2-13 as follows:
GBP is fixed for the VFOA,

$$\text{Gain A} * \text{Bandwidth A} = \text{Gain B} * \text{Bandwidth B}$$

GBP is not fixed for the CFOA,

$$\text{Gain A} * \text{Bandwidth A} \neq \text{Gain B} * \text{Bandwidth B}$$

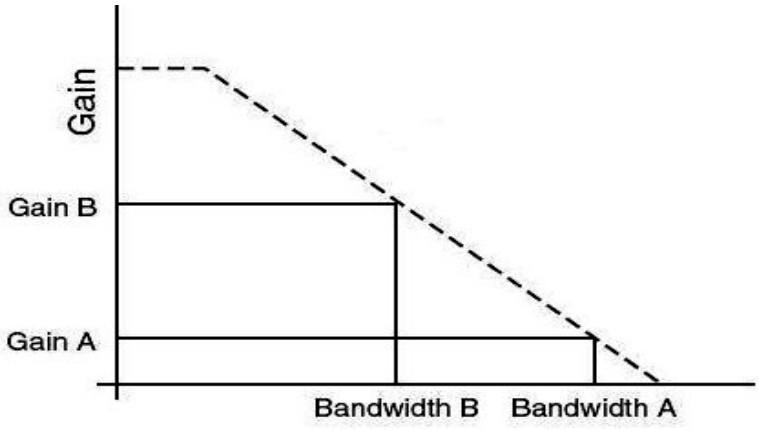


Figure 2-13: Gain and bandwidth relation [7]

2.6 Operational Floating Conveyor (OFC)

Toumazou et al. introduced the Operational Floating Conveyor (OFC) for the first time in 1991 [23]. A bipolar (BJT) implementation was presented using CFOA and current mirrors. Figure 2-14 illustrates the block diagram of OFC using CFOA and current mirrors. The feature of gain bandwidth independence as a current mode device was demonstrated.

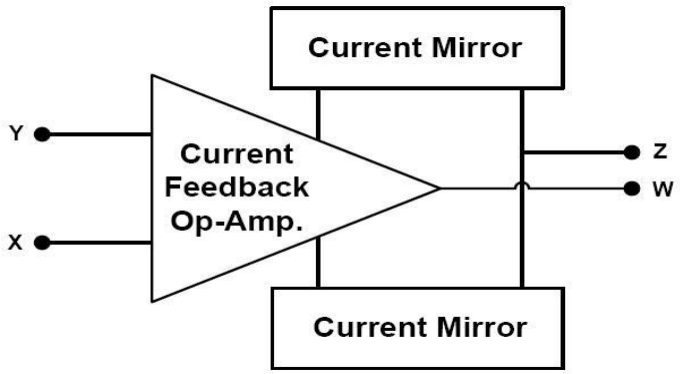


Figure 2-14: OFC block diagram using CFOA and current mirrors [23]

In 1994 Palmisano et al. redesigned the OFC and presented the CMOS realization shown in Figure 2-15 [24].

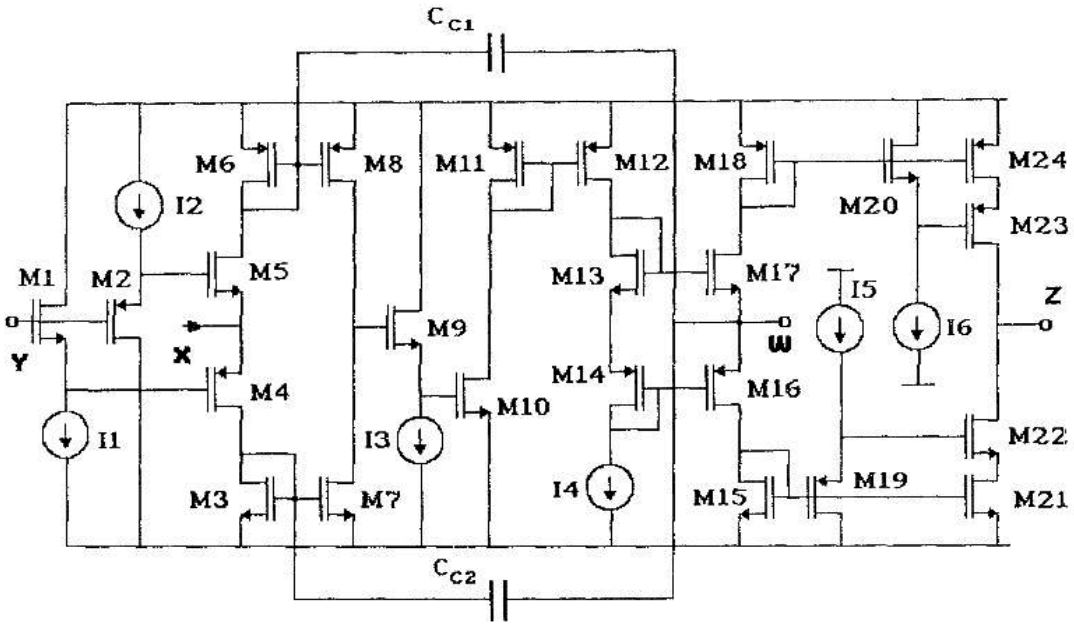


Figure 2-15: The first CMOS implementation of the OFC [24]

The OFC can be represented as a four terminal building block as shown in Figure 2-16. The OFC combines the transmission properties of both the Current Feedback Operational Amplifiers (CFOA) and the Current Conveyor (CCII) with additional current sensing capability (current output).

Figure 2-16: Block diagram representation of the OFC

The principle of operation of the OFC can be briefly summarized as follows: The voltage applied at terminal Y exactly appears at terminal X which represents the voltage following action at input terminals (X and Y). The current at terminal Y

equals zero due to the infinite input impedance of terminal Y. The voltage at terminal X is independent on the forced current I_X at the same terminal. The input impedance of terminal X is ideally zero. The input current at terminal X is multiplied by the open loop trans-impedance gain Zt to produce an output voltage at terminal W. Ideally, The output impedance of terminal W is zero while the output impedance of terminal Z is infinite. The current following action is accomplished by conveying the current I_W at output terminal W to the output terminal Z. This mechanism of operation can be represented using the following matrix form as:

$$\begin{bmatrix} V_X \\ I_Y \\ V_W \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ Zt & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_Y \\ I_W \\ V_Z \end{bmatrix} \tag{2-12}$$

The main high performance measures of the OFC are: high accuracy in voltage and current transfer, wide input voltage and current ranges, high open loop trans-impedance gain and wide bandwidth for voltage and current transfer. The OFC can be used for many applications like analog amplifiers and active filters [26].

The OFC can be implemented using different realizations. The same approach of these realizations will be used to implement the designs proposed in this thesis. Additional realizations other than the one shown in Figure 2-14 are explained as follows: The first realization can be obtained by using two CCII+ and one non inverting trans-impedance amplifier as shown in Figure 2-17 [24-26]. Figures 2-15 and 2-18 display two schematic diagrams for the OFC based on this realization.

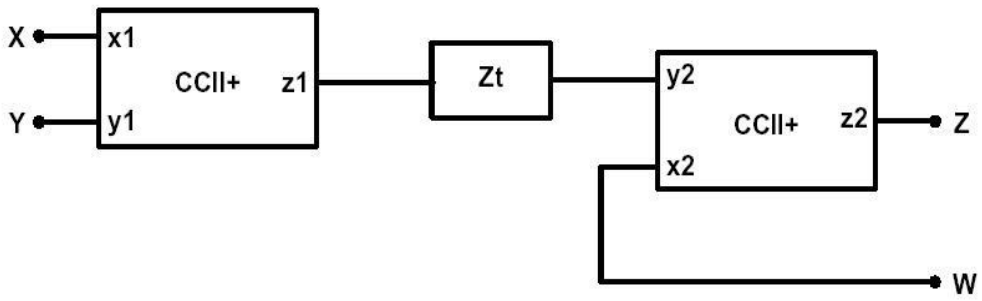


Figure 2-17: Block diagram of the first realization of OFC [24-26]

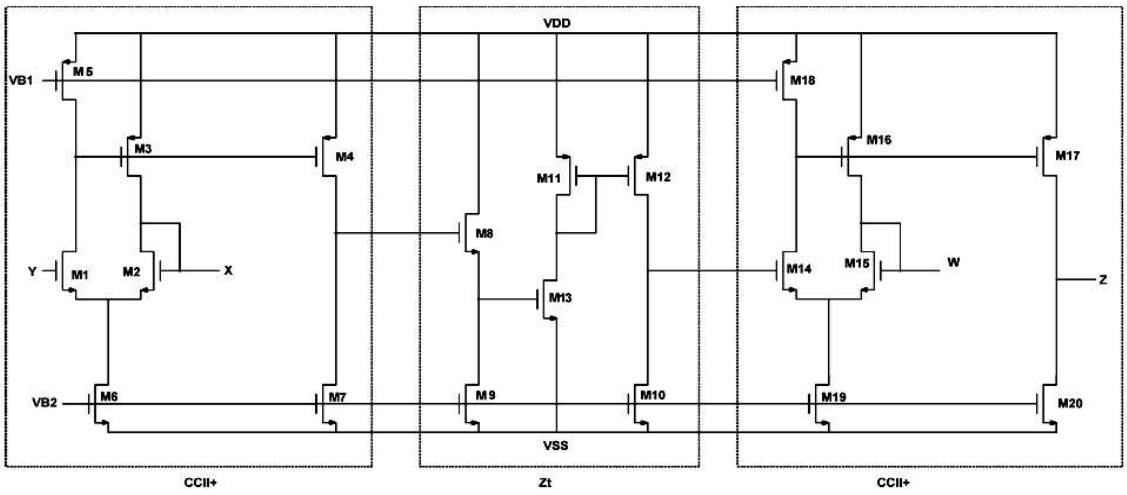


Figure 2-18: Schematic diagram of the OFC first realization of OFC [26]

The required voltage following action between input terminals (X and Y) is achieved by the first CCII+. The input current at terminal X is multiplied by the trans-impedance amplifier gain (Zt) to provide terminal W output voltage. The required current following action between output terminals (W and Z) is achieved by the second CCII+.

The second realization is obtained by using one CCII+, one non-inverting trans-impedance amplifier and one current follower as shown in Figure 2-19 [26]. The required voltage following action between input terminals (X and Y) is achieved by the CCII+. The input current at terminal X is multiplied by the trans-impedance amplifier gain (Zt) to provide terminal W output voltage. The required current following action between output terminals (W and Z) is achieved by the current follower.

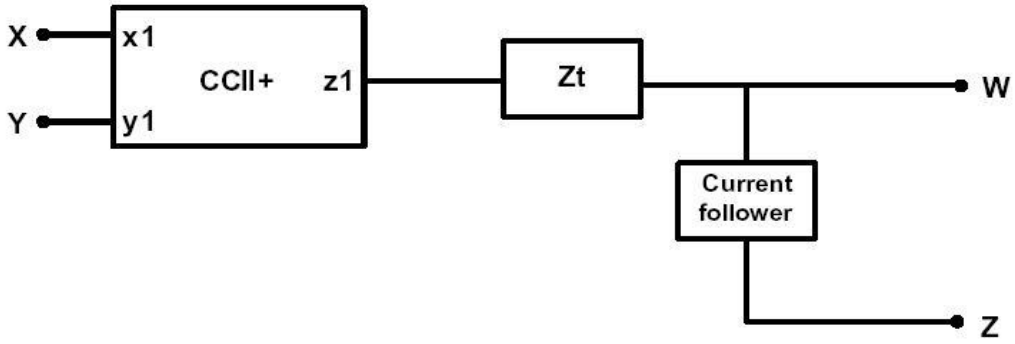


Figure 2-19: Block diagram of the second realization of OFC [26]

The third realization is obtained by using one CCII-, one inverting trans-impedance amplifier and one current follower as shown in Figure 2-20 [26]. The required voltage following action between input terminals (X and Y) is achieved by the CCII-. The input current at terminal X is multiplied by the trans-impedance amplifier gain (-Zt) to provide terminal W output voltage. The required current following action between output terminals (W and Z) is achieved by the current follower. Figures 2-21 displays a schematic diagrams for the OFC based on this realization.

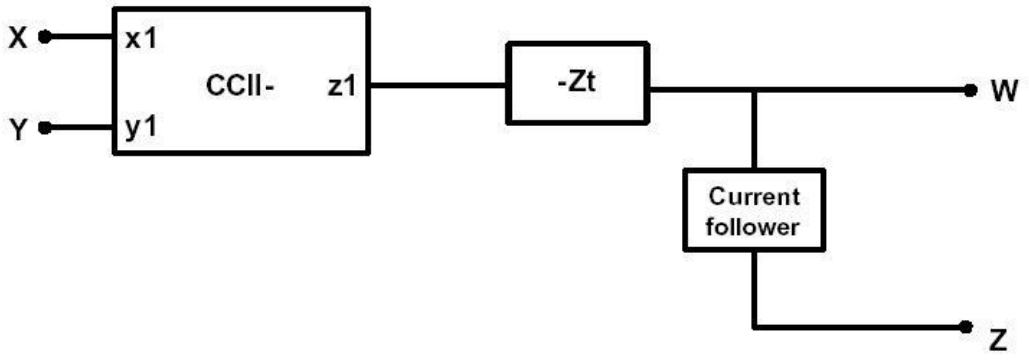


Figure 2-20: Block diagram of the third realization of OFC [26]

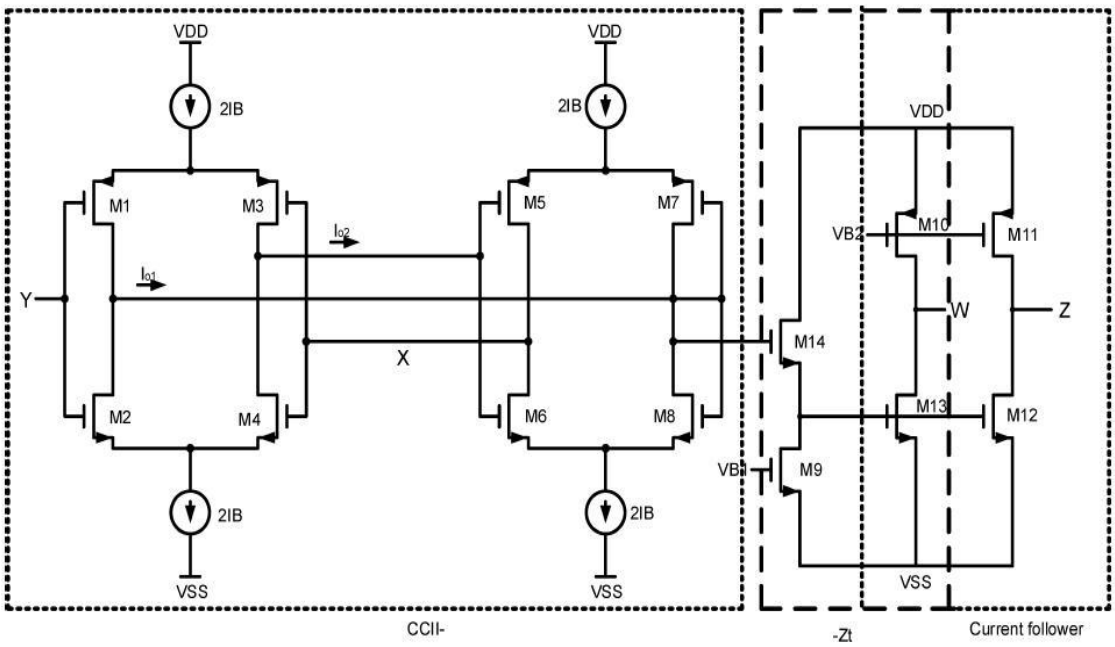


Figure 2-21: Schematic diagram of the OFC third realization of OFC [26]

2.7 Operational Floating Current Conveyor (OFCC)

The Operational Floating Current Conveyor was introduced by Khan et al. in 1994 [28]. Khan made some modification to the OFC to produce the OFCC as a new building block. Figure 2-22 shows the first OFCC implementation based on the BJT technology by Khan et al. Figure 2-24 displays one of the CMOS realizations of the OFCC [31].

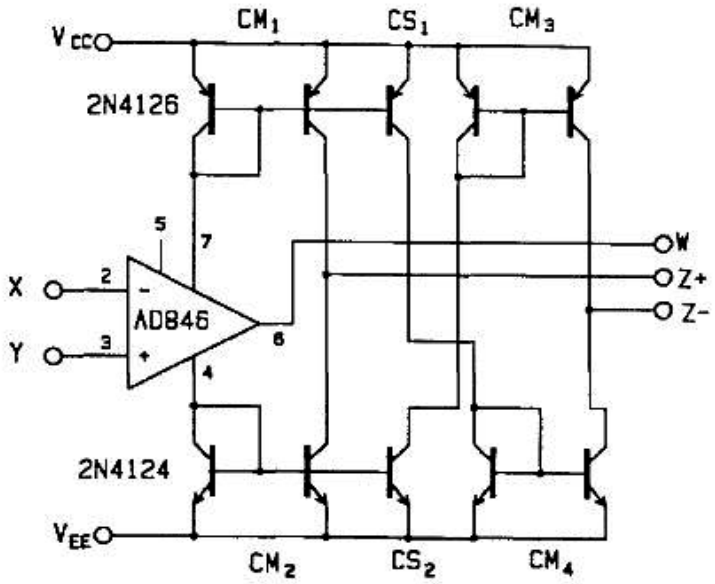


Figure 2-22: The first implementation of the OFCC [28]

The OFCC can be represented as a five terminal building block as shown in Figure 2-23. The OFCC has the same transmission properties of the OFC with additional current output to increase the device capabilities.

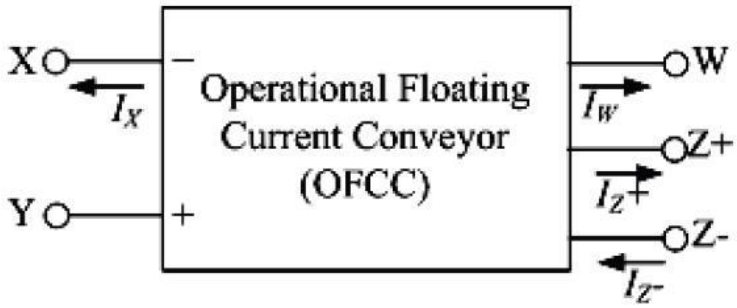


Figure 2-23: Block diagram representation of the OFCC [30]

The principle of operation of the OFCC can be briefly summarized as follows: The voltage applied at terminal Y exactly appears at terminal X which represents the voltage following action at input terminals (X and Y). The current at terminal Y equals zero due to the infinite input impedance of terminal Y. The voltage at terminal X is independent on the forced current I_X at the same terminal. The input impedance of terminal X is ideally zero. The input current at terminal X is multiplied by the open loop trans-impedance gain Zt to produce an output voltage at terminal W. Ideally, The output impedance of terminal W is zero while the output impedance of Z+ and Z- terminals are infinite. The current I_W is conveyed in-phase to the output terminal Z+ and conveyed out of phase to the output terminal Z-. This represents the current following action at output terminals (W, Z+ and Z-). This mechanism of operation can be represented using the following matrix form as:

$$\begin{bmatrix} I_Y \\ V_X \\ V_W \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & Zt & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ I_W \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \quad (2\text{-}13)$$

The main high performance measures of the OFCC are: high accuracy in voltage and current transfer, wide input voltage and current ranges, high open loop trans-impedance gain and wide bandwidth for voltage and current transfer. The OFCC can be used for many applications like analog amplifiers and active filters [29].

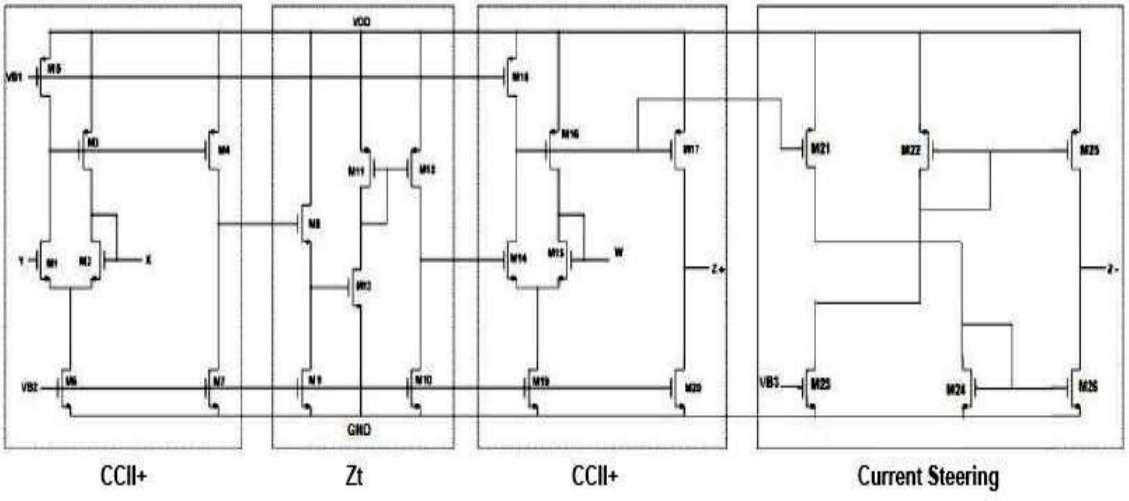


Figure 2-24: CMOS realization of the OFCC [31]

Chapter 3: The Proposed FD-OFC

3.1 Introduction

This Chapter introduces the novel concept along with a proposed schematic diagram for the model of the Fully Differential Operational Floating conveyor (FD-OFC) as an extension of the Operational Floating Conveyor (OFC) circuit [25,26] that is reviewed in Chapter 2. This extension is achieved using two different realizations/designs.

For the first time, the proposed FD-OFC concept and designs are introduced as an 8 (4x4) port general purpose analog building block as shown in Figure 3-1. The fully differential action offered by the proposed designs can be employed in numerous analog and/or hybrid (analog/digital) VLSI applications, particularly where a high noise rejection ratio is desired. Furthermore, the proposed designs can operate under low biasing conditions and exhibit wide bandwidth. It's shown via simulations that the proposed concept and circuit designs are perfectly suitable for low power – high speed application. A detailed analysis will be discussed within this chapter.

Figure 3-1: An 8 (4x4) port representation of the proposed FD-OFC

3.2 The FD-OFC transfer matrix

As shown in Figure 3-1, from a block diagram viewpoint, the FD-OFC has twice as much number of terminals as those in the conventional OFC which results in the operation in the fully differential mode; hence its name. Accordingly, the ideal I/O

terminal behavior can be expressed in terms of a transfer matrix of the FD-OFC "$T^{(FD\text{-}OFC)}(\omega)$" as follows:

$$\begin{bmatrix} V_{xd}(\omega) \\ I_{yd}(\omega) \\ V_{wd}(\omega) \\ I_{zd}(\omega) \end{bmatrix} = T^{(FD-OFC)}(\omega) \begin{bmatrix} I_{xd}(\omega) \\ V_{yd}(\omega) \\ I_{wd}(\omega) \\ V_{zd}(\omega) \end{bmatrix} \tag{3-1}$$

where ω is the angular frequency (ω = 2 π f).

The (i ,j) entry of the FD-OFC transfer matrix "$T^{(FD\text{-}OFC)}$" is given by:

$$\left(T^{(FD-OFC)}\right)_{ij} = I_2 \otimes \left(T^{(OFC)}\right)_{ij} \tag{3-2}$$

Where, I_2 is the a 2x2 identity matrix, $T^{(OFC)}$ is the transfer matrix of the OFC and $\otimes$ is the Kronicker product.

$$I_2 = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \tag{3-3}$$

$$T^{(OFC)}(\omega) = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ Z_t & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \tag{3-4}$$

$$\begin{aligned} I_{xd} &= \begin{bmatrix} I_{x1} & I_{x2} \end{bmatrix}^T, \quad I_{yd} = \begin{bmatrix} I_{y1} & I_{y2} \end{bmatrix}^T, \\ I_{wd} &= \begin{bmatrix} I_{w1} & I_{w2} \end{bmatrix}^T, \quad I_{zd} = \begin{bmatrix} I_{z1} & I_{z2} \end{bmatrix}^T, \\ V_{xd} &= \begin{bmatrix} V_{x1} & V_{x2} \end{bmatrix}^T, \quad V_{yd} = \begin{bmatrix} V_{y1} & V_{y2} \end{bmatrix}^T, \\ V_{wd} &= \begin{bmatrix} V_{w1} & V_{w2} \end{bmatrix}^T, \quad V_{zd} = \begin{bmatrix} V_{z1} & V_{z2} \end{bmatrix}^T \end{aligned} \tag{3-5}$$

And $[.]^T$ denotes the matrix transpose operator.

Accordingly, the FD-OFC transfer matrix can be expanded as follows:

$$T^{(FD-OFC)}(\omega)=\begin{bmatrix} 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ Z_t & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & Z_t & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \end{bmatrix} \quad (3\text{-}6)$$

It should be noted that $T^{(FD\text{-}OFC)}(\omega)$ implicitly depends on the angular frequency through the frequency dependence of Z_t.

3.3 The main building block

The main building block that will be used for the two realizations/designs of the Fully Differential Operational Floating Conveyer (FD-OFC) is the inverting Fully Differential second generation Current Conveyor (FDCCII-).

3.3.1 The selected FDCCII- circuit

The FDCCII- circuit, which is used here as the main building block, is shown in Figure 3-2. The strength of this selected design [21,22] is that it exhibits wider bandwidth and a rail to rail input voltage dynamic range with a smaller number of transistors (smaller area). Table 3-1 shows a comparison between the selected design of the FDCCII and other designs that have been presented in the literature review (Chapter 2) [16-22].

The selected FDCCII- design was originally published [21,22] using 350 nm technology and the supply value was 1.5 Volt as shown in Figure 3-2. In this work the supply voltage is reduced to 1.2 Volt and the technology used is 130 nm.

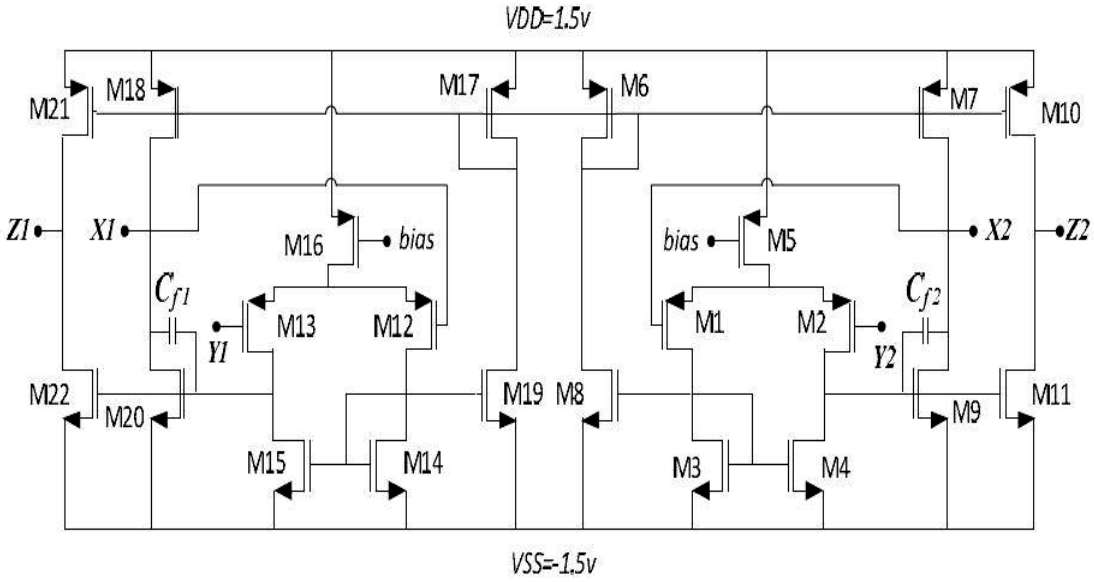


Figure 3-2: Schematic diagram representation of the FDCCII- [21,22]

Structure	Technology	Supply Voltage	I/P voltage dynamic Range	3-dB Frequency (B.W)	No. of Transistors
[16]	1.2 μm	± 1.5 v	-200 mv to +200 mv	10 MHz	36
[17]	0.35 μm	± 1.5 v	NA	26 MHz	36
[20]	0.35 μm	± 1.25 v	-390 mv to +390 mv	2.02 GHz	48
[19] Real. 1	0.35 μm	± 1.5 v	-1.5 v to +0.44 v	116 MHz	22
[19] Real. 2	0.35 μm	± 1.5 v	-1.5 v to +1.5 v	232 MHz	32
[19] Real. 3	0.35 μm	± 1.5 v	-1.5 v to +1.5 v	206 MHz	24
[18]	90 nm	+ 1.2 v	-450 mv to 450 mv	254 MHz	52
Implemented [21,22]	130 nm	± 1.2 v	-1.2 v to +1.2 v	800 MHz	22

Table 3-1: Comparison between different structures of the FDCCII

3.3.2 Simulation results of the FDCCII-

The FDCCII- circuit is simulated using UMC 130 nm CMOS-based technology kit in Cadence environment. The simulation starts by characterizing each of the MOSFET transistors used in the constructed model of the FDCCII- as required by Cadence. The entire circuit is simulated using 1.2 Volt biasing conditions. The transistor specification of the FDCCII- is illustrated in Table 3-2.

Transistor Name	Transistor Aspect Ratio W/L (µm/µm)
M7-M10-M18-M21	63.7/0.39
M9-M11-M20-M22	55.9/0.39
M5-M16	20.8/0.13
M1-M2-M12-M13	11.96/0.13
M3-M4-M14-M15	5.9/0.13
M6-M17	11.18/0.13
M8-M19	7.54/0.13

Table 3-2: Transistor aspect ratio for the FDCCII-

Figure 3-3 shows the DC characteristic between the X and Y terminals' differential voltages (V_{xd} vs. V_{yd}) which proves the voltage following relation between these terminals. Y terminal differential voltage (V_{yd}) is swept from -1.2 v to 1.2 v.

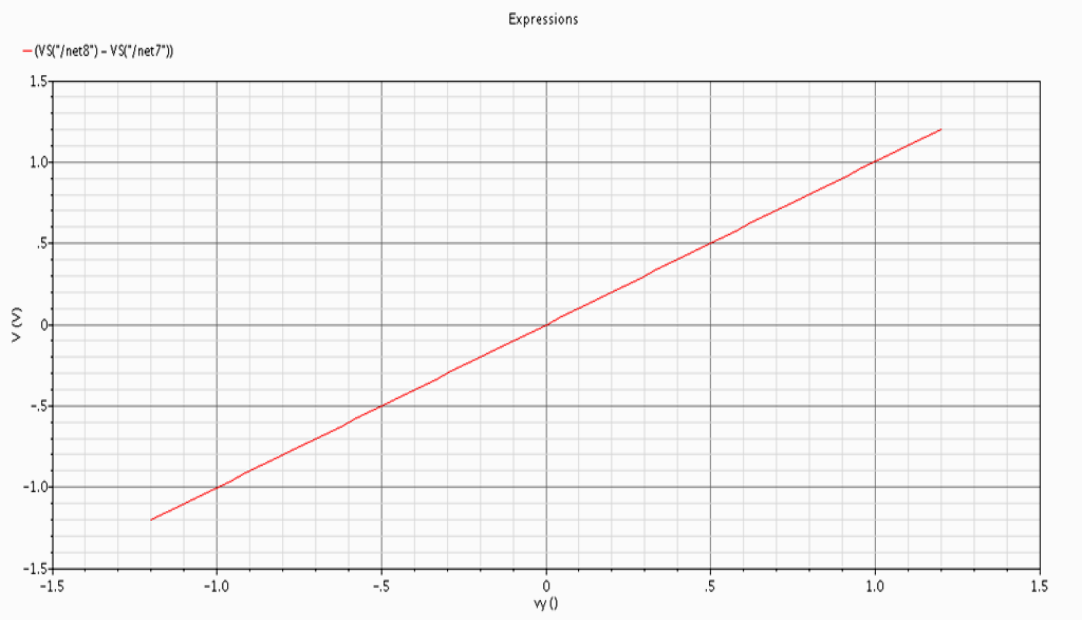


Figure 3-3: DC characteristics between X & Y terminals' voltages (Vxd vs.Vyd)

Figure 3.4 shows the DC characteristics between the X and Z terminals' currents (Iz vs. Ix) which proves the current following relation between these terminals. For inverting FDCCII, the current relation slope is negative. X terminal current (Ix) is swept from -1 mA to 1mA.

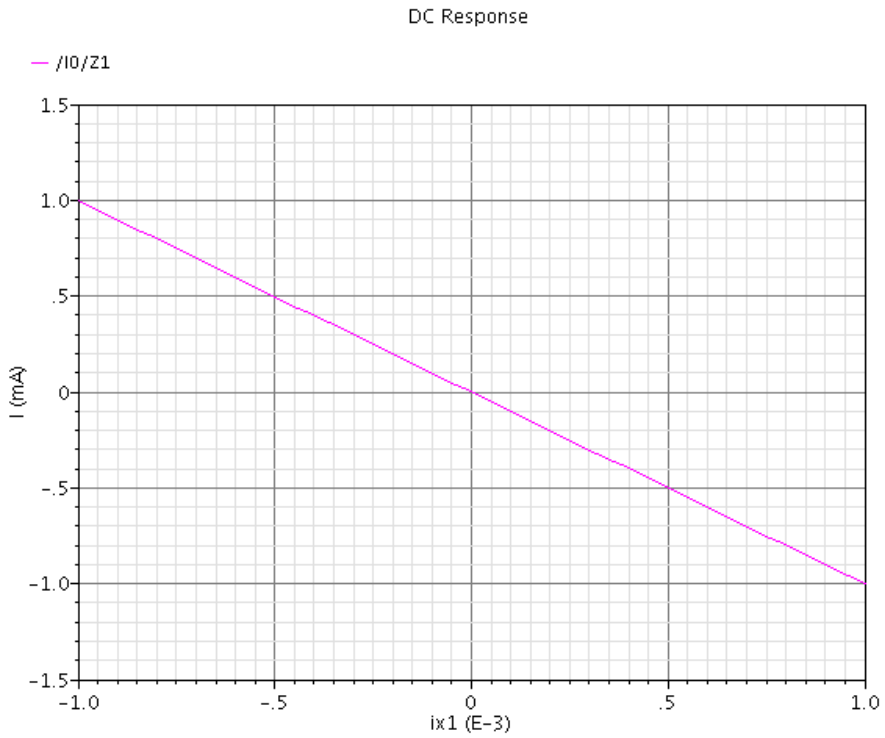
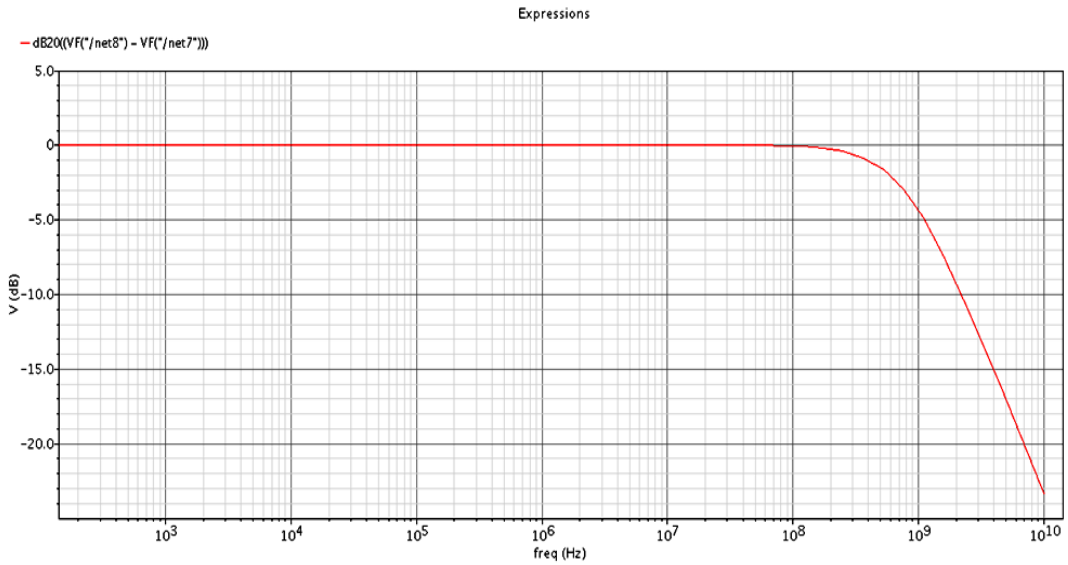
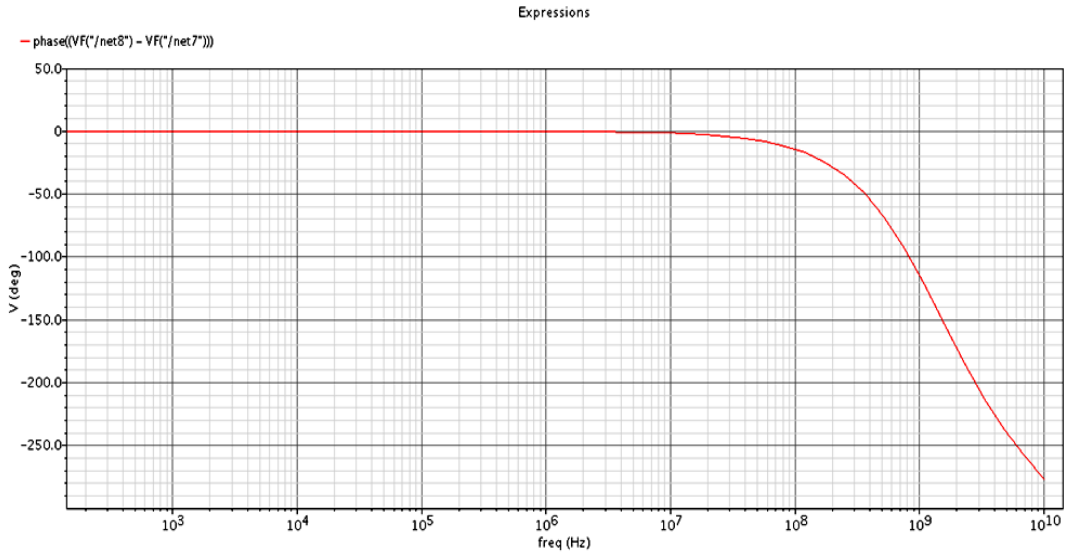


Figure 3-4: DC characteristics between X and Z terminals' currents (Iz vs.Ix)

Figures 3-5 (a) & (b) show the AC characteristics between the X and Y terminals' differential Voltages (V_{xd} / V_{yd}). Figure 3-5(a) plots the magnitude frequency response between X and Y terminals' Voltages (in dB) while, Figure 3-5(b) plots the phase frequency response between X and Y terminals' voltages (in degrees).



(a)

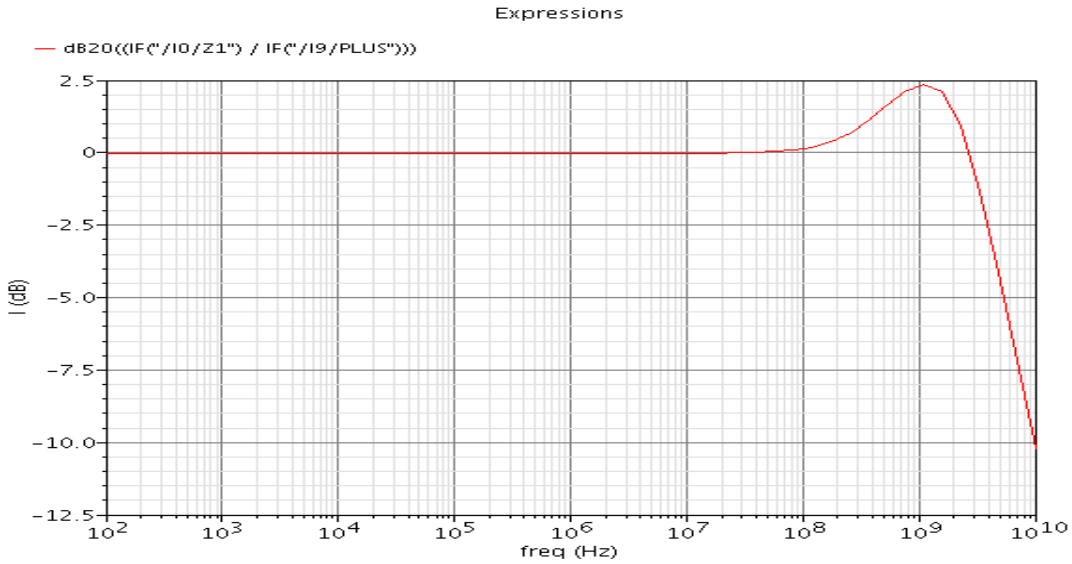


(b)

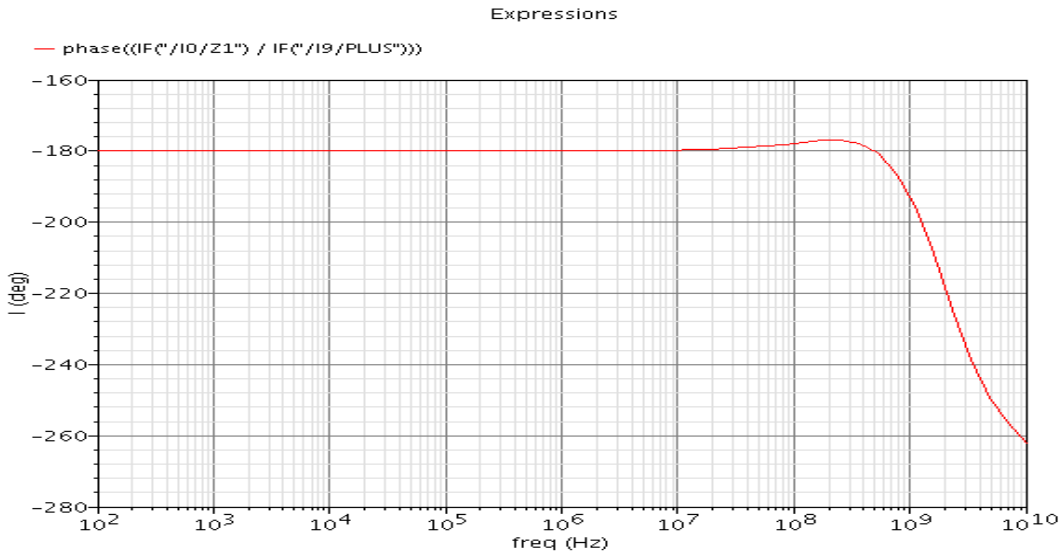
Figure 3-5: AC characteristics between X and Y terminals' Voltages (Vxd / Vyd)

(a) Magnitude frequency response (b) Phase frequency response

Figures 3-6 (a) & (b) show the AC characteristics between the Z and X terminals' Currents (Iz / Ix). Figure 3-6 (a) plots the magnitude frequency response between Z and X terminals' Currents (in dB) while, Figure 3-6 (b) plots the phase frequency response between Z and X terminals' currents (in degrees).



(a)



(b)

Figure 3-6: AC characteristics between Z and X terminals' currents (Iz / Ix)

(a) Magnitude frequency response (b) Phase frequency response

3.4 The first proposed FD-OFC (Realization 1)

This section presents the first proposed FD-OFC as an extension of the conventional OFC circuit. This extension is achieved by cascading two FDCCII-'s via two non-inverting trans-impedance amplifiers, of Zt gain each. Figure 3-7 illustrates this concept via block diagram representation, while the schematic diagram representations for the FDCCII- and the trans-impedance amplifier are shown in Figures 3-2 and 3-8, respectively. The complete circuit of the first proposed FD-OFC is shown in Figure 3-9.

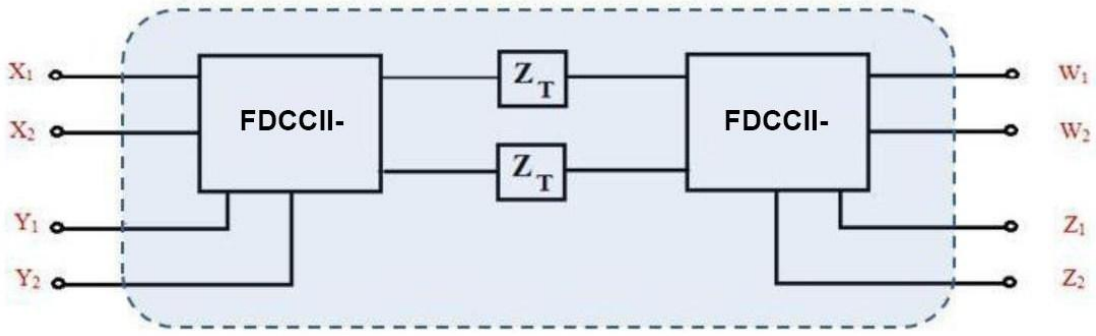


Figure 3-7: Building blocks of the first proposed FD-OFC

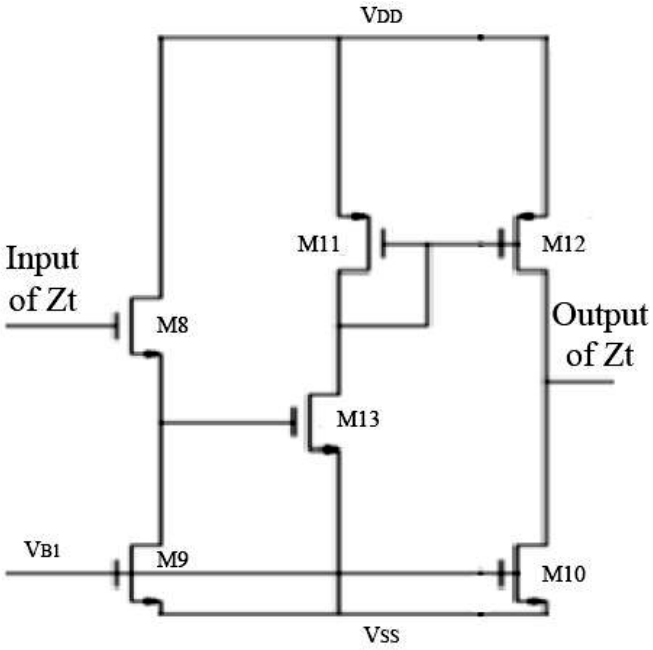


Figure 3-8: Schematic diagram representation of the trans-impedance amplifier [26]

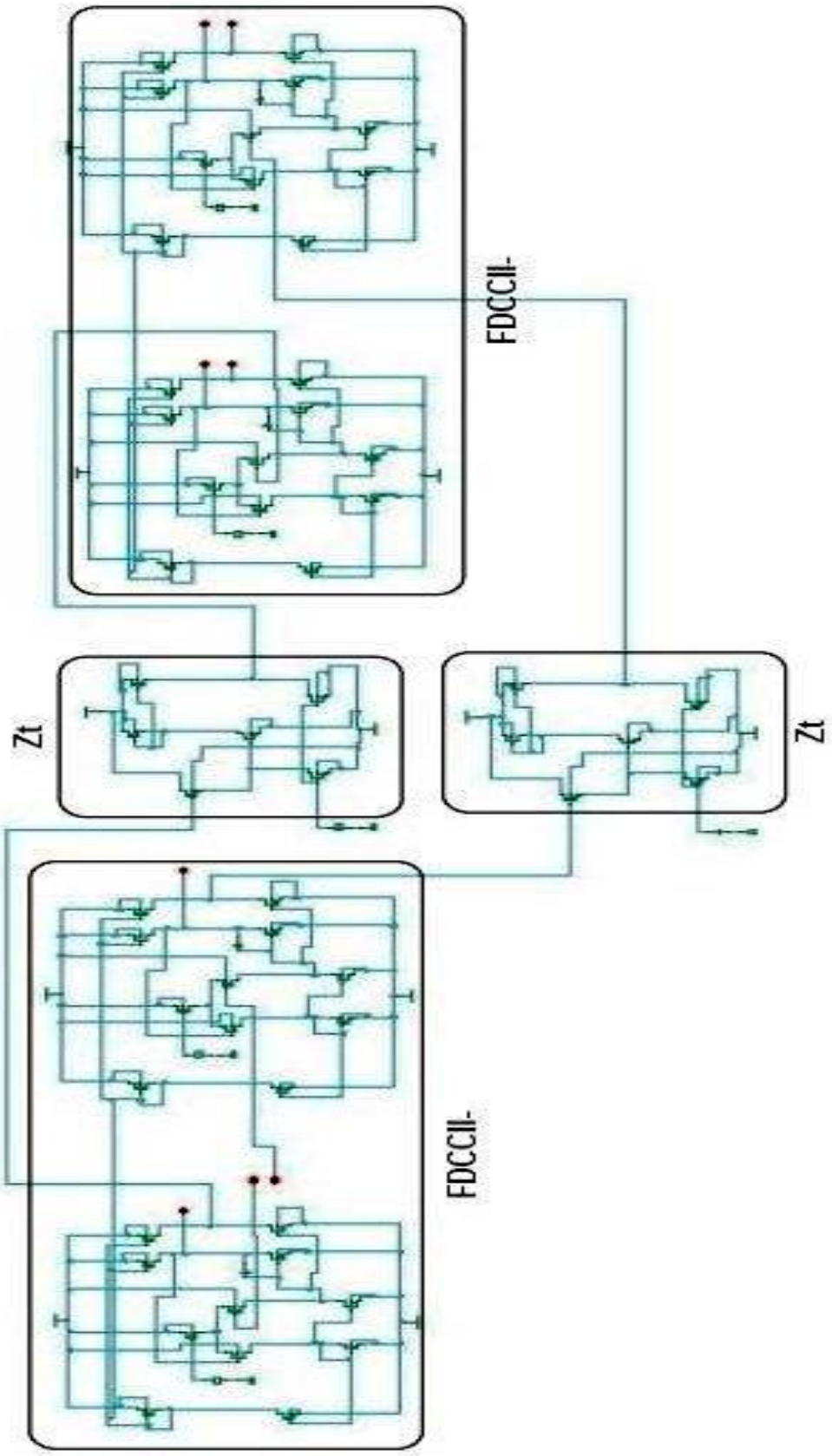


Figure 3-9: The complete circuit of the first proposed FD-OFC

3.4.1 Circuit description

The first realization is done by using two FDCCII- which are coupled together using two non-inverting trans-impedance amplifier of Zt gain each. The first FDCCII- is used to perform the required differential voltage following action between X and Y terminals (input ports). The second FDCCII- is used to perform the required differential current following action between Z and W terminals (output ports). The output voltage at terminal W is obtained by multiplying the input current at terminal X by the trans-impedance amplifier gain Zt.

The operation of the trans-impedance amplifier can be described as follows: After terminal X input current is mirrored through the FDCCII-, it will flow in the equivalent parasitic impedance of M8 gate terminal. This current produces a voltage on the gate terminal of M8. This voltage is then amplified through three stages M8, M13 and M12. These three transistors M8, M13 and M12 are connected in common drain, common source and common source configurations, respectively. The output voltage of the trans-impedance amplifier is applied to the input terminal of the second FDCCII- to be conveyed to produce the output voltage at terminal W.

The input terminals $Y_1(1)$ and $Y_2(1)$ of the first FDCCII- are assigned to two of the **FD-OFC** inputs ($\mathbf{Y_1}$ and $\mathbf{Y_2}$), while the other input terminals $X_1(1)$ and $X_2(1)$ of the first FDCCII- are assigned to the other **FD-OFC** input terminals as $\mathbf{X_1}$ and $\mathbf{X_2}$. The output terminals of the first FDCCII- $Z_1(1)$ and $Z_2(1)$ are connected to the input of the two trans-impedance amplifiers Zt. The input terminals $Y_1(2)$ and $Y_2(2)$ of the second FDCCII- are connected to the outputs of the two trans-impedance amplifiers Zt. The other input terminals $X_1(2)$ and $X_2(2)$ of the second FDCCII- are assigned to two of the **FD-OFC** outputs ($\mathbf{W_1}$ and $\mathbf{W_2}$), while the output terminals $Z_1(2)$ and $Z_2(2)$ of the second FDCCII- are assigned to the other **FD-OFC** output terminals as $\mathbf{Z_1}$ and $\mathbf{Z_2}$.

3.4.2 Simulation results of the first proposed FD-OFC

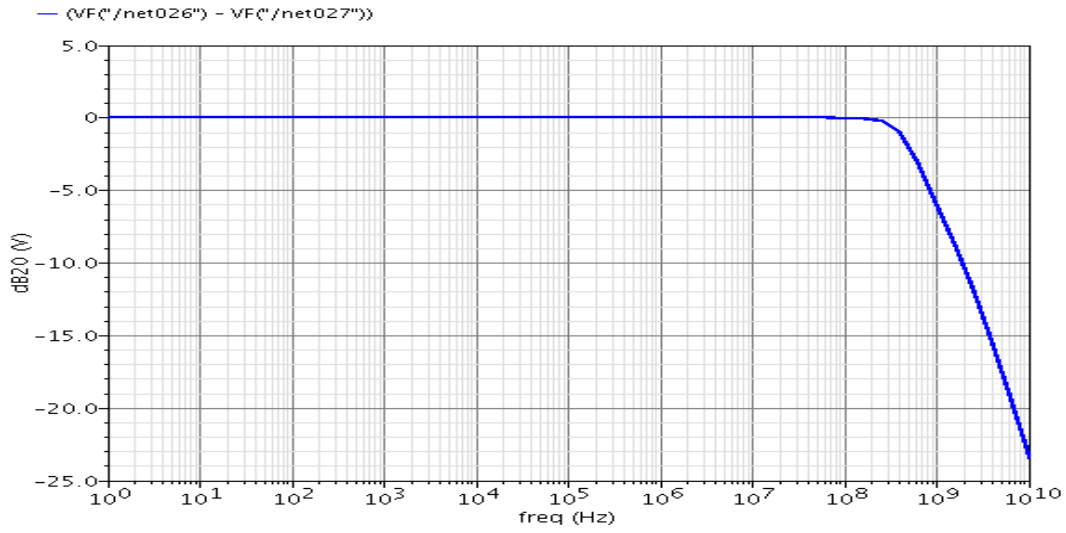
This section is devoted to present numerical results that validate the analysis provided in the previous section as well as the workability of the proposed design. The proposed FD-OFC circuit is simulated using UMC 130 nm CMOS-based technology kit in Cadence environment. The simulation starts by characterizing each of the MOSFET transistors, displayed in Figures 3-2 and 3-7, via their geometrical structural design parameters given in Table 3-2 and 3-3 as required by Cadence. The entire circuit is simulated using 1.2 Volt biasing conditions.

Transistor Name	Transistor Aspect Ratio W/L (µm/µm)
M8	10.4/0.65
M9-M13	26/0.65
M10	5.2/0.65
M11-M12	13/0.65

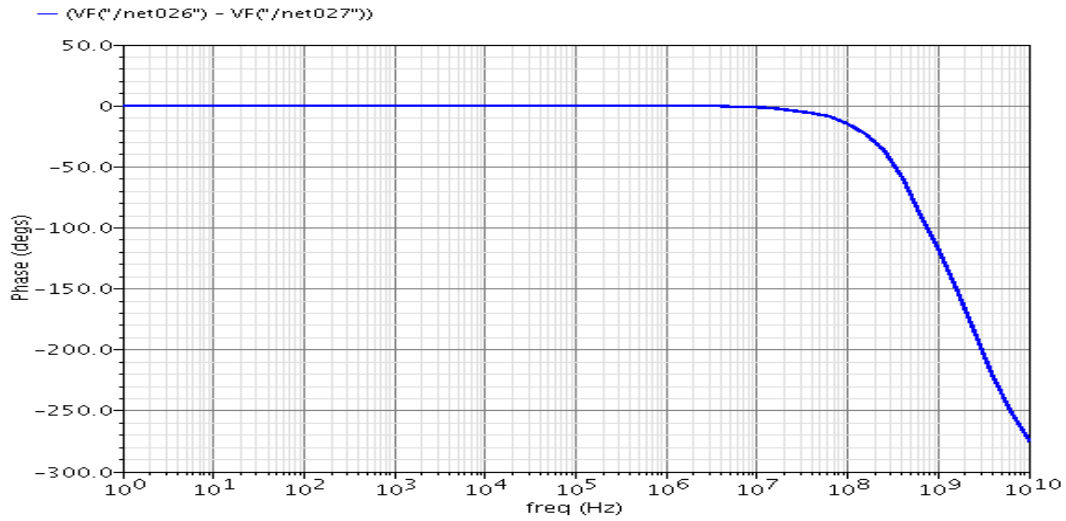
Table 3-3: Transistor aspect ratio for the trans-impedance amplifier (Zt)

Figures 3-10, 3-11 and 3-12 show the frequency response (magnitude and phase). In all figures, it's clear that the frequency responses are essentially flat for frequencies ranging from 0 to more than 100 MHz for magnitude frequency response and to more than 10 MHz for phase frequency response. This flat response confirms the suitability of the proposed FD-OFC for various switching speeds of analog applications. In general, it can be correctly concluded that the bandwidth of the proposed FD-OFC is about 600 MHz.

Figures 3-10 (a) & (b) show the AC characteristics between the X and Y terminals' differential Voltages (V_{xd} / V_{yd}). Figure 3-10(a) plots the magnitude frequency response between X and Y terminals' Voltages (in dB) while, Figure 3-10(b) plots the phase frequency response between X and Y terminals' voltages (in degrees). Clearly these two figures confirm the voltage following action between the two terminals in the differential form as well as distortion-free transmission between the two terminals. The 3-dB frequency (Bandwidth) for open circuit voltage transfer gain is 600 MHz.



(a)

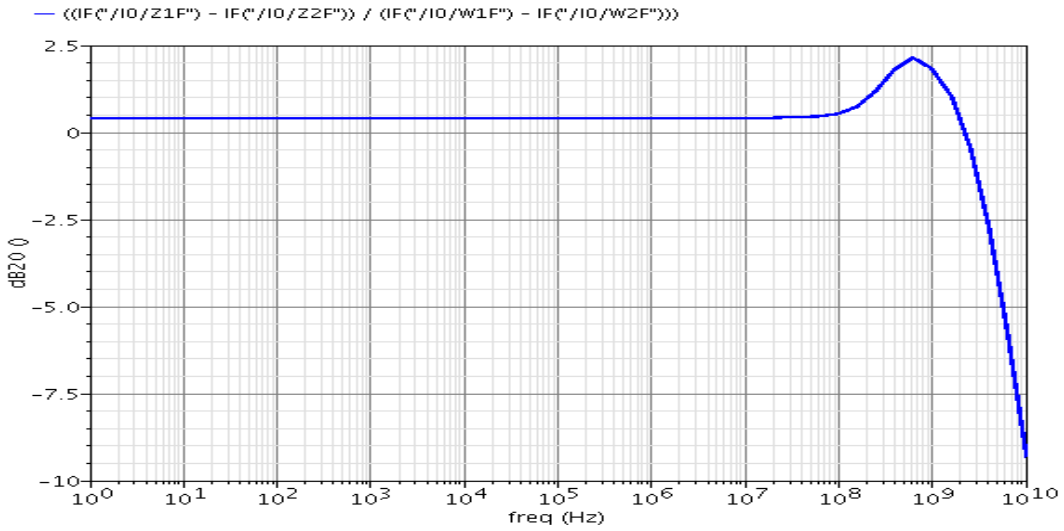


(b)

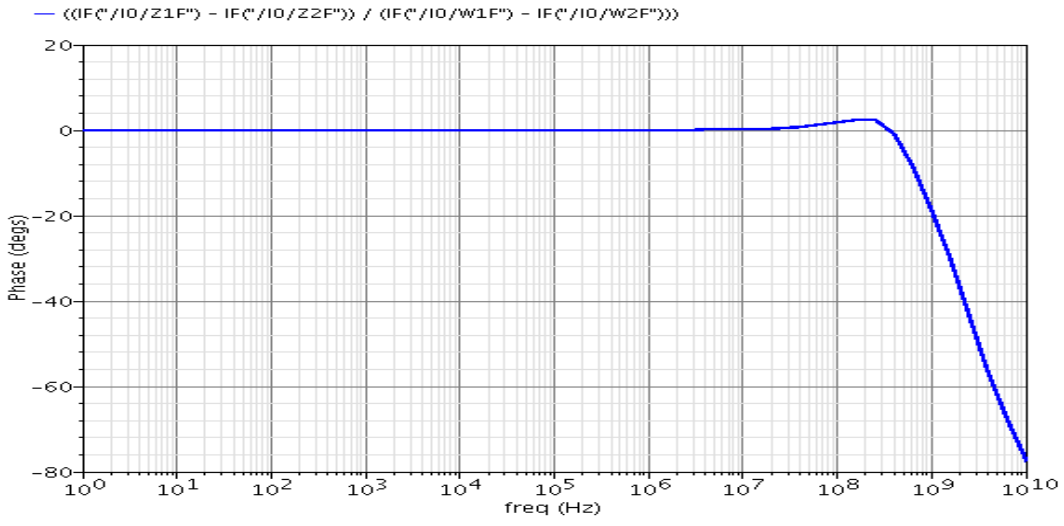
Figure 3-10: AC characteristics between X and Y terminals' voltages (Vxd / Vyd)

(a) Magnitude frequency response (b) Phase frequency response

Figures 3-11 (a) & (b) show the AC characteristics between the Z and W terminals' differential currents (I_{zd} / I_{wd}). Figure 3-11(a) plots the magnitude frequency response between Z and W terminals' currents (in dB) while, Figure 3-11(b plots the phase frequency response between Z and W terminals' currents (in degrees). These two figures confirm the validity of approximating a current following action between the two terminals in the differential form except for a gain of only 0.44 dB, corresponding to a constant offset of 0.05 from an expected unity gain. The phase shift between both terminals is zero for frequencies ranging from 0 to about 20 MHz.



(a)

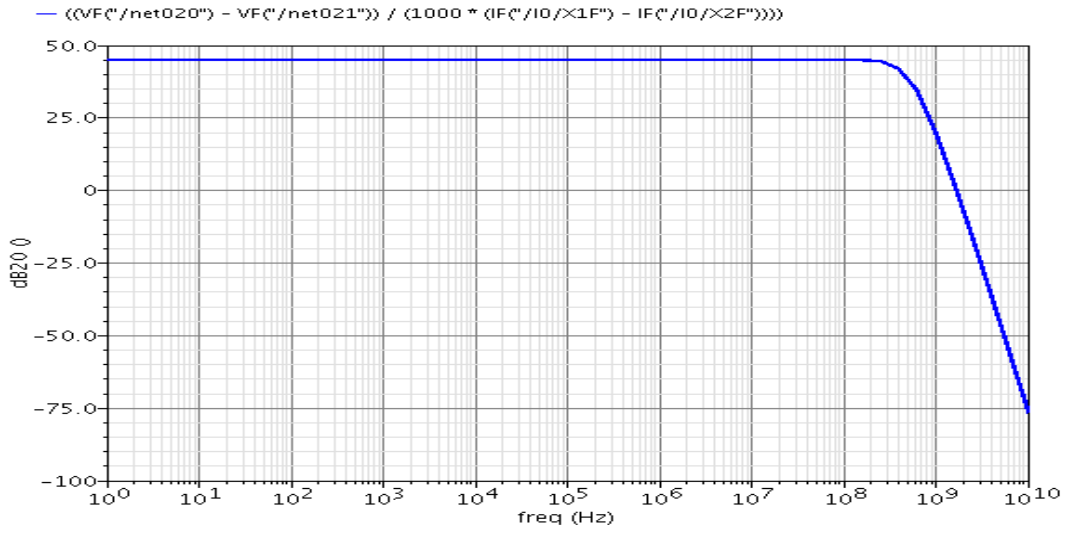


(b)

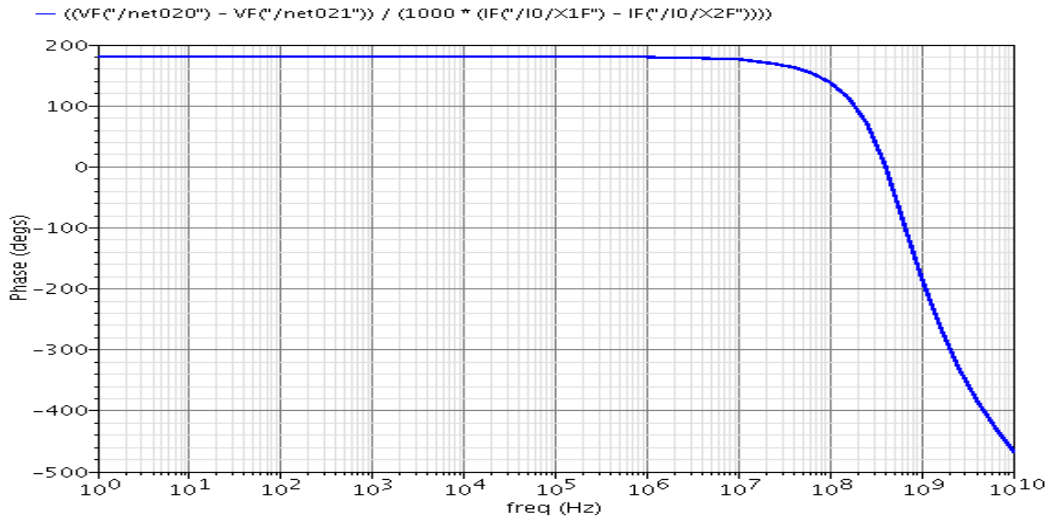
Figure 3-11: AC characteristics between Z and W terminals' currents (Izd / Iwd)

(a) Magnitude frequency response (b) Phase frequency response

Figures 3-12 (a) & (b) show the AC characteristics between the differential voltage at terminal W and the differential current at terminal X (V_{wd} / I_{xd}). Figure 3-12(a) plots the magnitude frequency response between W and X terminals (in dB) while Figure 3-12(b) plots the phase frequency response between W and X terminals (in degrees). The open loop trans-impedance gain is invariant and equal to 44.5 dB for AC signals having frequencies up to about 100 MHz. Again, the phase response preserves its constancy with zero degree up to about one decade less than the magnitude response.



(a)



(b)

Figure 3-12: AC characteristics between W and X terminals (Vwd / Ixd)

(a) Magnitude frequency response (b) Phase frequency response

3.5 The second proposed FD-OFC (Realization 2)

This section presents the second proposed FD-OFC as an extension of the conventional OFC circuit. This extension is achieved by cascading the two output terminals (Z terminals) of the FDCCII- to two current followers via two inverting trans-impedance amplifiers of -Zt gain each. Figure 3-13 illustrates this concept via block diagram representation, while the schematic diagram representations for the FDCCII- and the current follower integrated with the trans-impedance amplifier are shown in Figures 3-2 and 3-14, respectively. The complete circuit of the second proposed FD-OFC is shown in Figure 3-15.

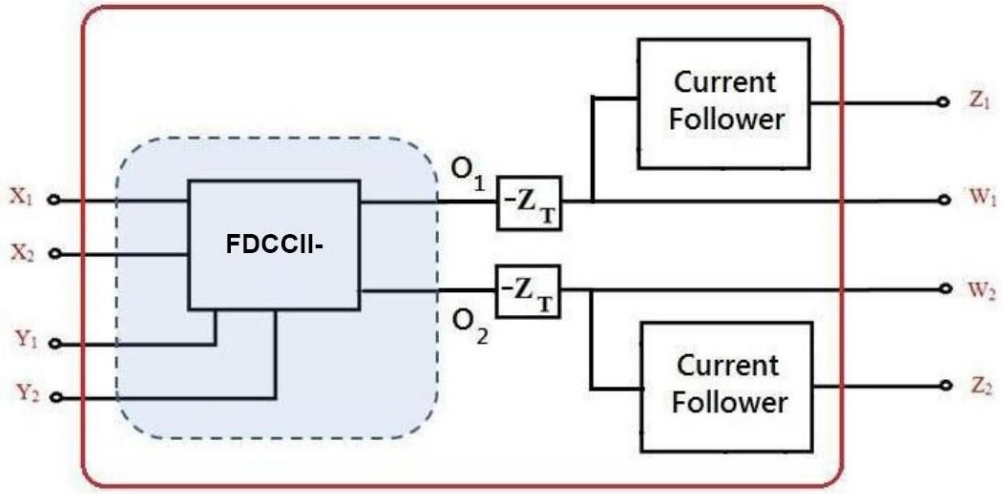


Figure 3-13: Building blocks of the second proposed FD-OFC

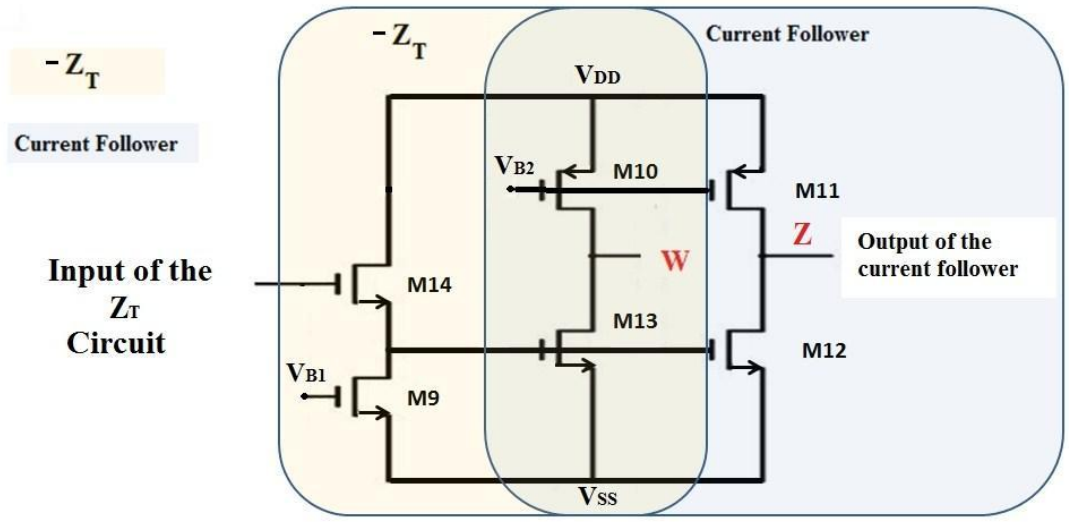


Figure 3-14: Schematic diagram representation of the integrated inverting trans-impedance amplifier and the current follower [26]

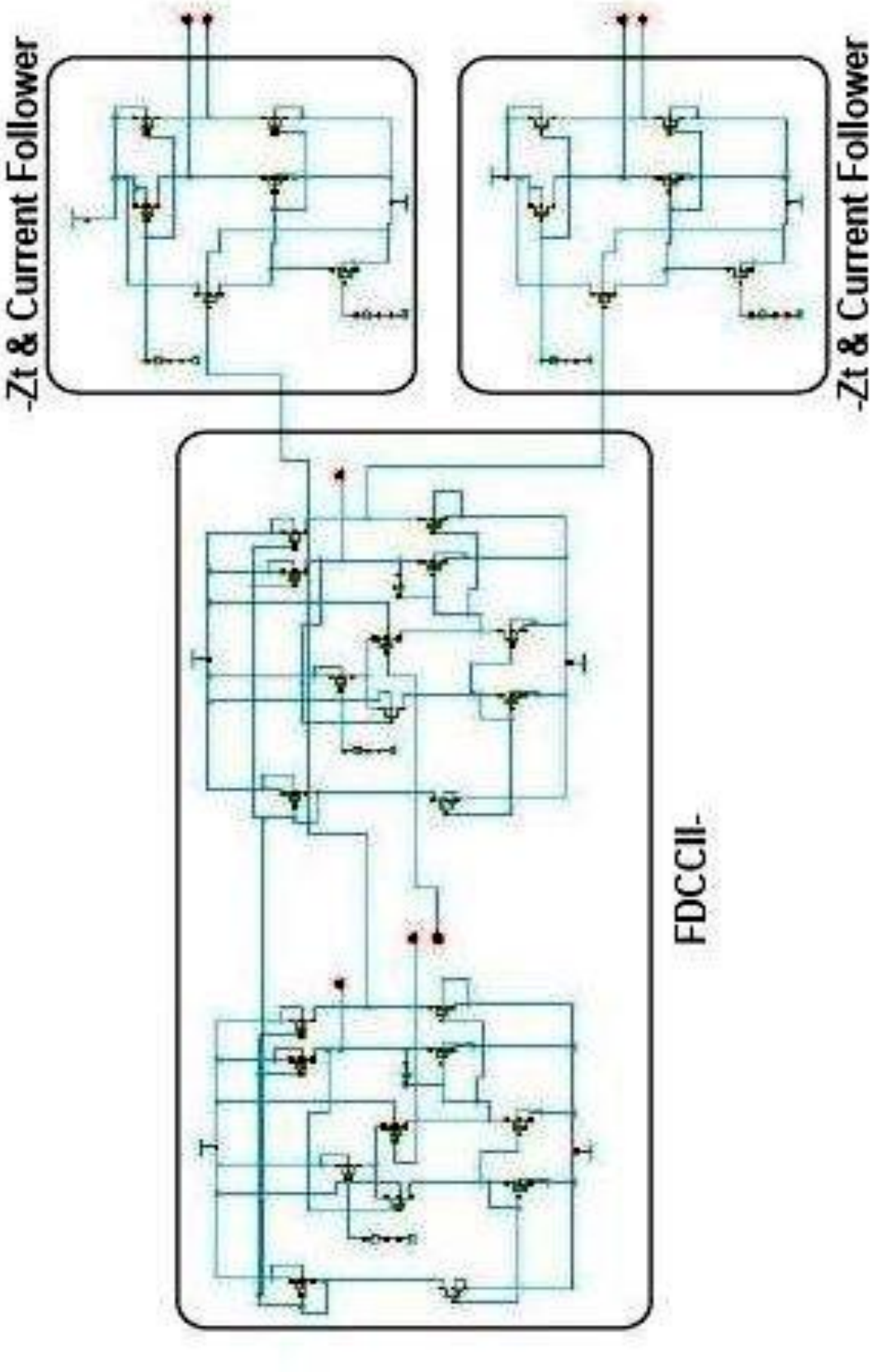


Figure 3-15: The complete circuit of the second proposed FD-OFC

3.5.1 Circuit description

The second realization is done by using one FDCCII- connected to two inverting trans-impedance amplifiers, of -Zt gain each, that are integrated with two current followers. The FDCCII- is used to perform the required differential voltage following action between X and Y terminals (input ports). The output voltage at terminal W is obtained by multiplying the input current at terminal X by the trans-impedance amplifier gain -Zt. The current followers are connected, to the inverting trans-impedance amplifiers, such that the required differential current following action is achieved between Z and W terminals (output ports).

The operation of the trans-impedance amplifier can be described as follows: After terminal X input current is mirrored through the FDCCII-, it will flow in the equivalent parasitic impedance of M9 gate terminal. This current produces a voltage on the gate terminal of M9. This voltage is then amplified through two stages M14, M13 to produce the output voltage at terminal W. These two transistors M14 and M13 are connected in common drain and common source configurations, respectively. The current is conveyed to the output terminal Z through the current followers.

The input terminals Y_1 and Y_2 of the FDCCII- are assigned to two of the **FD-OFC** inputs ($\mathbf{Y_1}$ and $\mathbf{Y_2}$), while the other input terminals X_1 and X_2 of the FDCCII- are assigned to the other **FD-OFC** input terminals as $\mathbf{X_1}$ and $\mathbf{X_2}$. The output terminals of the FDCCII- Z_1 and Z_2 are connected to the input of the two inverting trans-impedance amplifiers Zt. The outputs of the two inverting trans-impedance amplifiers are assigned to two of the **FD-OFC** outputs ($\mathbf{W_1}$ and $\mathbf{W_2}$), while the outputs of the two current followers are assigned to the other **FD-OFC** output terminals as $\mathbf{Z_1}$ and $\mathbf{Z_2}$.

3.5.2 Simulation results of the second proposed FD-OFC

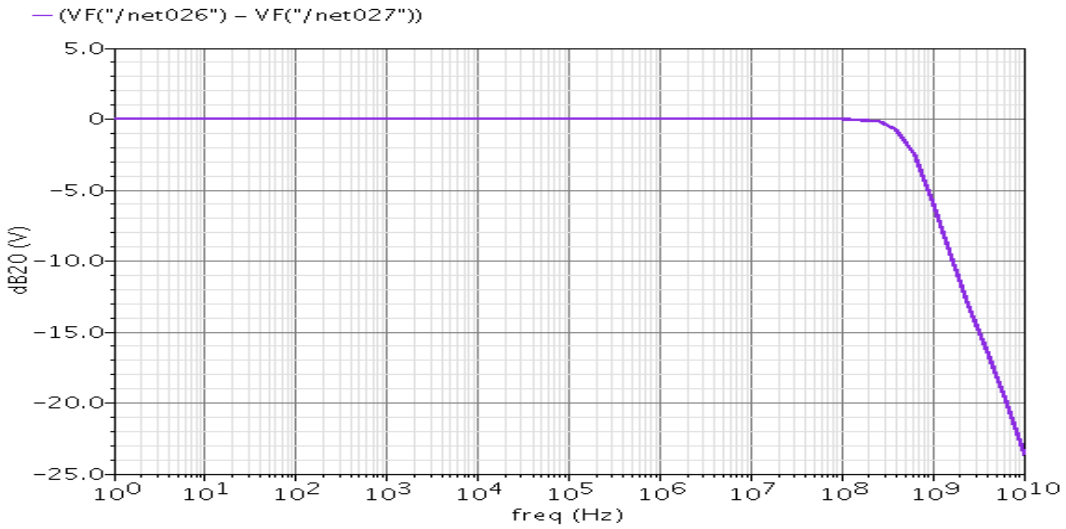
This section is devoted to present numerical results that validate the analysis provided in the previous section as well as the workability of the proposed design. The proposed FD-OFC circuit is simulated using UMC 130 nm CMOS-based technology kit in Cadence environment. The simulation starts by characterizing each of the MOSFET transistors, displayed in Figures 3-2 and 3-14, via their geometrical structural design parameters given in Table 3-2 and 3-4 as required by Cadence. The entire circuit is simulated using 1.2 Volt biasing conditions.

Transistor Name	Transistor Aspect Ratio W/L (µm/µm)
M9-M12-M13	1.3/0.65
M10-M11	2.6/0.65
M14	2.6/0.13

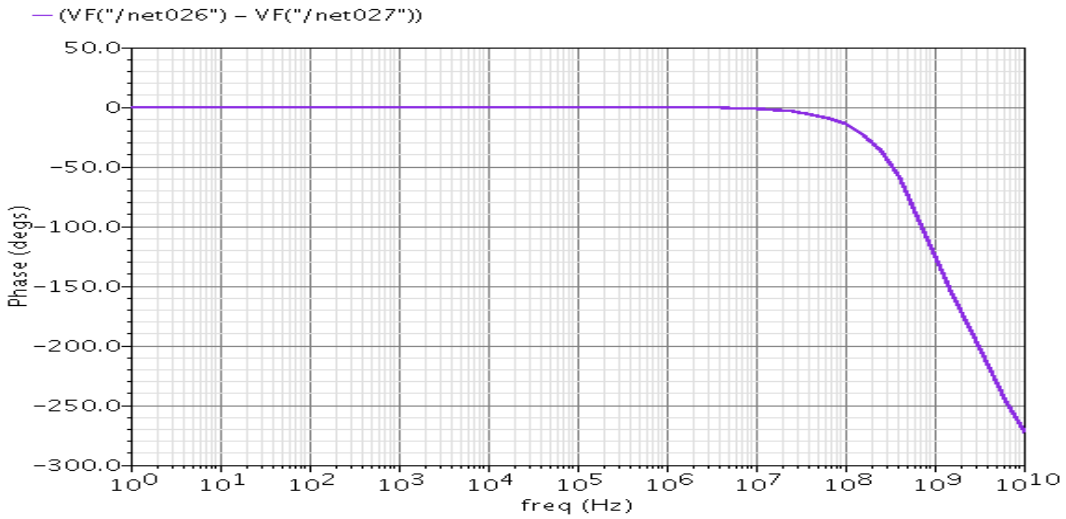
Table 3-4: Transistor aspect ratio for the inverting trans-impedance amplifier (-Zt) and the current follower

Figures 3-16, 3-17 and 3-18 show the frequency response (magnitude and phase). In all figures, it's clear that the frequency responses are essentially flat for frequencies ranging from 0 to more than 100 MHz for magnitude frequency response and to more than 10 MHz for phase frequency response. This flat response confirms the suitability of the proposed FD-OFC for various switching speeds of analog applications.

Figures 3-16 (a) & (b) show the AC characteristics between the X and Y terminals' differential Voltages (V_{xd} / V_{yd}). Figure 3-16(a) plots the magnitude frequency response between X and Y terminals' Voltages (in dB) while, Figure 3-16(b) plots the phase frequency response between X and Y terminals' voltages (in degrees). Clearly these two figures confirm the voltage following action between the two terminals in the differential form as well as distortion-free transmission between the two terminals. The 3-dB frequency (Bandwidth) for open circuit voltage transfer gain is 600 MHz.



(a)

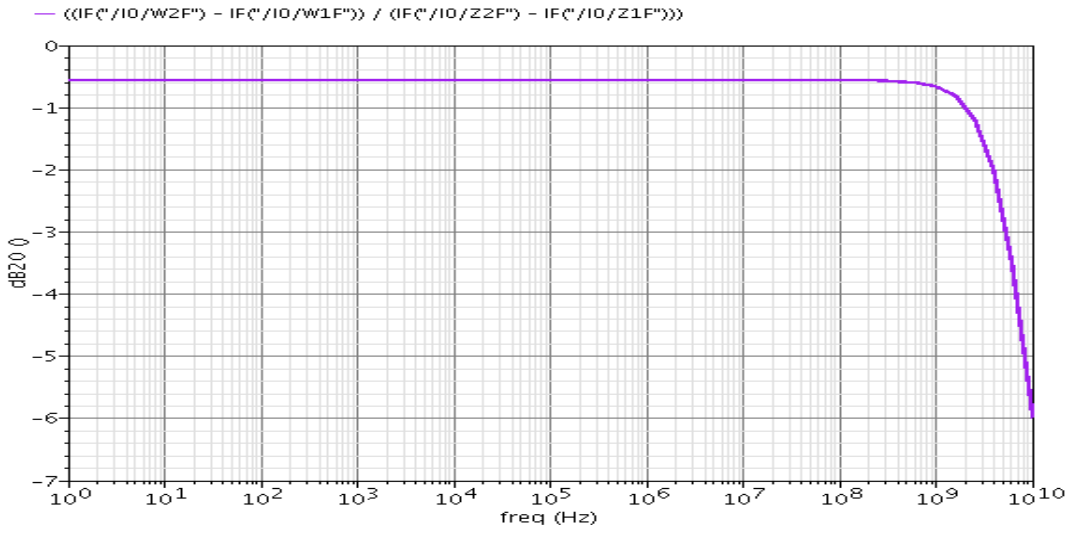


(b)

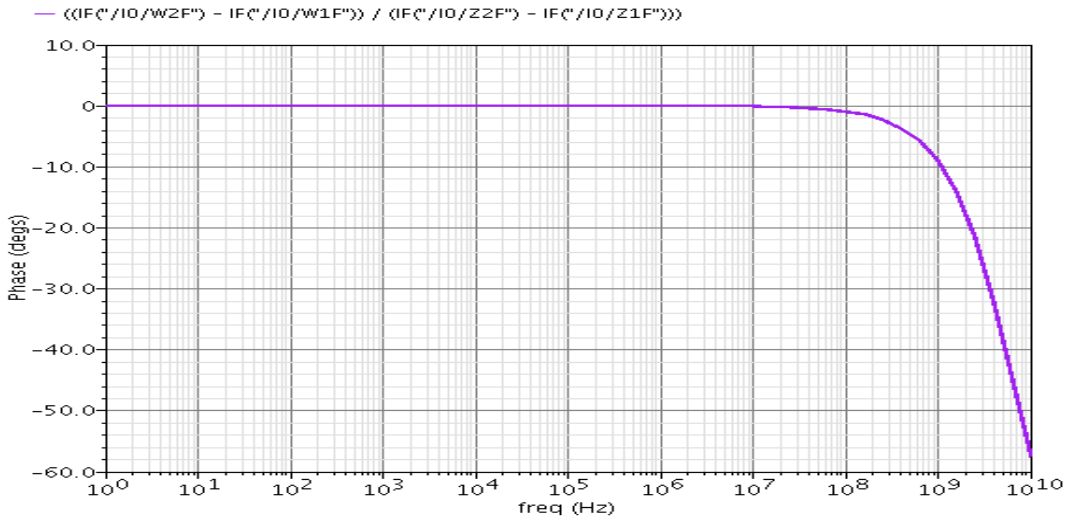
Figure 3-16: AC characteristics between X and Y terminals' voltages (Vxd / Vyd)

(a) Magnitude frequency response (b) Phase frequency response

Figures 3-17 (a) & (b) show the AC characteristics between the Z and W terminals' differential currents (I_{wd} / I_{zd}). Figure 3-17(a) plots the magnitude frequency response between Z and W terminals' currents (in dB) while, Figure 3-17(b plots the phase frequency response between Z and W terminals' currents (in degrees). These two figures confirm the validity of approximating a current following action between the two terminals in the differential form except for a gain of only - 0.56 dB, corresponding to a constant offset of 0.062 from an expected unity gain. The phase shift between both terminals is zero for frequencies ranging from 0 to about 20 MHz.



(a)

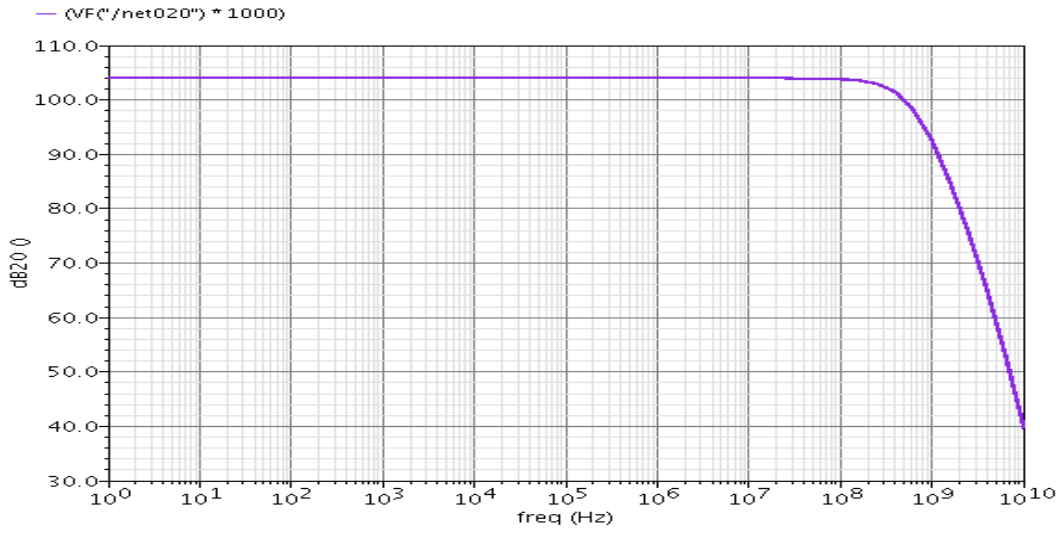


(b)

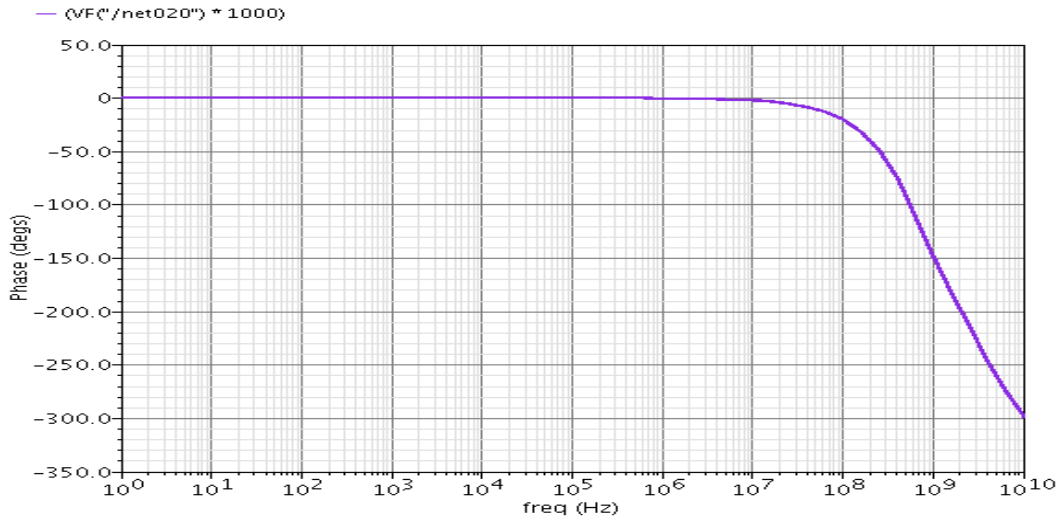
Figure 3-17: AC characteristics between Z and W terminals' currents (Iwd / Izd)

(a) Magnitude frequency response (b) Phase frequency response

Figures 3-18 (a) & (b) show the AC characteristics between the differential voltage at terminal W and the differential current at terminal X (V_{wd} / I_{xd}). Figure 3-18(a) plots the magnitude frequency response between W and X terminals (in dB) while, Figure 3-18(b) plots the phase frequency response between W and X terminals (in degrees). The open loop trans-impedance gain is constant and equal to 104 dB for AC signals having frequencies up to about 100 MHz. Again, the phase response preserves its constancy with zero degree up to about one decade less than the magnitude response.



(a)



(b)

Figure 3-18: AC characteristics between W and X terminals (Vwd / Ixd)

(a) Magnitude frequency response (b) Phase frequency response

3.6 Comparison between the two proposed realizations

A performance comparison is done between the two proposed FD-OFC realizations/designs. This comparison in shown in Table 3-5 based on different parameters like 3-dB frequency (B.W), DC open loop trans-impedance gain, number of transistors (area) and power dissipation.

Parameter	Proposed Realization 1	Proposed Realization 2
Technology	130 nm	130 nm
Supply voltage	1.2 V	1.2 V
3-dB frequency for open circuit voltage transfer gain	600 MHz	600 MHz
The used building blocks (numbers and types)	Two “FDCCII-” & Two “Zt”	One “FDCCII-”, Two “-Zt” , &Two “Current Followers”
Number of transistors	56	34
DC open loop trans-impedance gain	44.5 dB	104 dB
Power dissipation	28.36 mW	19.71 mW

Table 3-5: Comparison between the two proposed realizations of the FD-OFC

Based on the above results, it’s clear that the second realization/design has the following advantages. It has less number of transistors (34 transistors instead of 56 for the first design) which leads to the reduction of device area and power consumption. Less power dissipation 19.71 mW (compared to 28.36 mW for the first design). Furthermore, It has higher DC open loop trans-impedance gain which is 104 dB (compared to 44.5 dB for the first design).

Chapter 4: FD-OFC Based Applications

4.1 Introduction

In this Chapter, the Fully Differential Operational Floating Conveyor (FD-OFC), as a novel general purpose analog building block, will be used to implement different applications. The FD-OFC combines the features of the conventional OFC with the advantages of fully differential signal processing like higher design flexibility and higher noise rejection. This differential action offered by the proposed designs can be employed in numerous analog and/or hybrid (analog/digital) VLSI applications. The FD-OFC exhibits a wide bandwidth at high gain values for these applications where this bandwidth is approximately gain independent.

The FD-OFC is used in applications while configured in closed loop implementation with current feedback from terminal W to terminal X. The presented applications in this chapter are: fully differential voltage amplifier, Non-inverting voltage amplifier, Inverting voltage amplifier, fully differential integrator, fully differential second generation current conveyor (FDCCII) and current mode instrumentation amplifier (CMIA).

4.2 Fully differential voltage amplifier

The voltage amplifier, as voltage controlled voltage source (VCVS), is one of the conventional OFC applications [26]. It can be configured as shown in Figure 4-1 to be fully differential voltage amplifier based on the FD-OFC. The input signal is applied differentially between the input terminals Y1 and Y2 while the output is taken differentially across the output terminals W1 and W2.

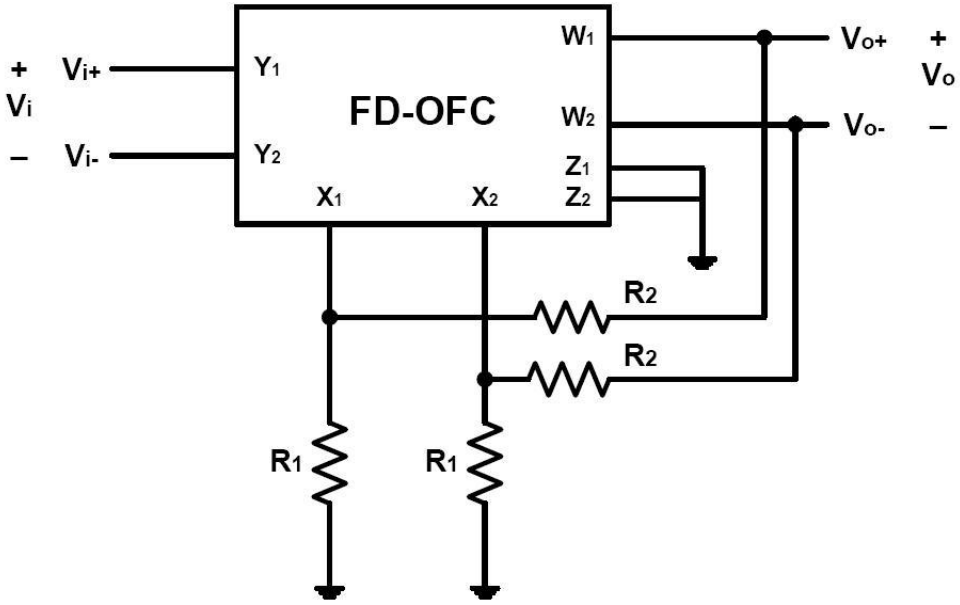


Figure 4-1: Fully differential voltage amplifier

The voltage gain (A_v) is given by:

$$A_V = \frac{V_O}{V_i} = 1 + \frac{R_2}{R_1} \tag{4-1}$$

The above expression can be derived as follows:

By applying KCL at terminal X1,

$$I_{X1} + \frac{V_{W1} - V_{X1}}{R_2} = \frac{V_{X1}}{R_1} \tag{4-2}$$

Substituting by

$$I_{X1} = \frac{V_{W1}}{Z_t(s)} \tag{4-3}$$

$$\frac{V_{W1}}{Z_t(s)} + \frac{V_{W1} - V_{X1}}{R_2} = \frac{V_{X1}}{R_1} \tag{4-4}$$

$$V_{W1}\left(1 + \frac{R_2}{Z_t(s)}\right) = V_{X1}\left(1 + \frac{R_2}{R_1}\right) \tag{4-5}$$

$$\because V_{X1} = V_{Y1} = V_{i+} \quad \& \quad V_{W1} = V_{O+} \tag{4-6}$$

$$V_{O+} = V_{W1} = V_{i+}\left(1+\frac{R_2}{R_1}\right)\frac{1}{\left(1+\frac{R_2}{Z_t(s)}\right)} \tag{4-7}$$

Similarly,

$$\because V_{X2} = V_{Y2} = V_{i-} \quad \& \quad V_{W2} = V_{O-} \tag{4-8}$$

$$V_{O-} = V_{W2} = V_{i-}\left(1+\frac{R_2}{R_1}\right)\frac{1}{\left(1+\frac{R_2}{Z_t(s)}\right)} \tag{4-9}$$

$$V_{O+} - V_{O-} = V_{W1} - V_{W2} = \left(V_{i+} - V_{i-}\right)\left(1+\frac{R_2}{R_1}\right)\frac{1}{\left(1+\frac{R_2}{Z_t(s)}\right)} \tag{4-10}$$

$$A_V = \frac{V_O}{V_i} = \frac{V_{O+} - V_{O-}}{V_{i+} - V_{i-}} = \left(1+\frac{R_2}{R_1}\right)\frac{1}{\left(1+\frac{R_2}{Z_t(s)}\right)} \tag{4-11}$$

$$A_V = \frac{V_O}{V_i} = \left(1+\frac{R_2}{R_1}\right)\varepsilon(s) \tag{4-12}$$

where ε(s) is the error function and can be expressed as:

$$\varepsilon(s) = \frac{1}{\left(1+\frac{R_2}{Z_t(s)}\right)} \tag{4-13}$$

Ideally, the trans-impedance gain Zt(s) is considered very large (infinite) which leads to a unity error function (i.e. $\varepsilon(s) \approx 1$).

$$A_V = \frac{V_O}{V_i} = 1+\frac{R_2}{R_1} \tag{4-14}$$

Generally, the finite trans-impedance gain Zt(s) can be expressed using the single pole (time constant) model as:

$$Z_t(s) = \frac{Z_{to}}{1 + \frac{s}{\omega_o}} \qquad (4\text{-}15)$$

where Z_{to} is the DC open loop trans-impedance gain and ω_o is the trans-impedance cut off frequency.

4.2.1 Circuit simulation

The fully differential voltage amplifier circuit is simulated using UMC 130 nm CMOS-based technology kit in Cadence environment. The entire circuit is simulated using the same transistor specification of the FD-OFC and 1.2 Volt biasing conditions.

The frequency response of different gains of the circuit (: $A_V = 1 + R_2/R_1$) is shown in Figure 4-2 using R_2 = 1 KΩ and R_1 = 10 Ω, 20 Ω, 100 Ω and 1 KΩ. It's clear that, the actual gain is much closer to the ideal gain for higher gain values and the bandwidth is approximately gain independent.

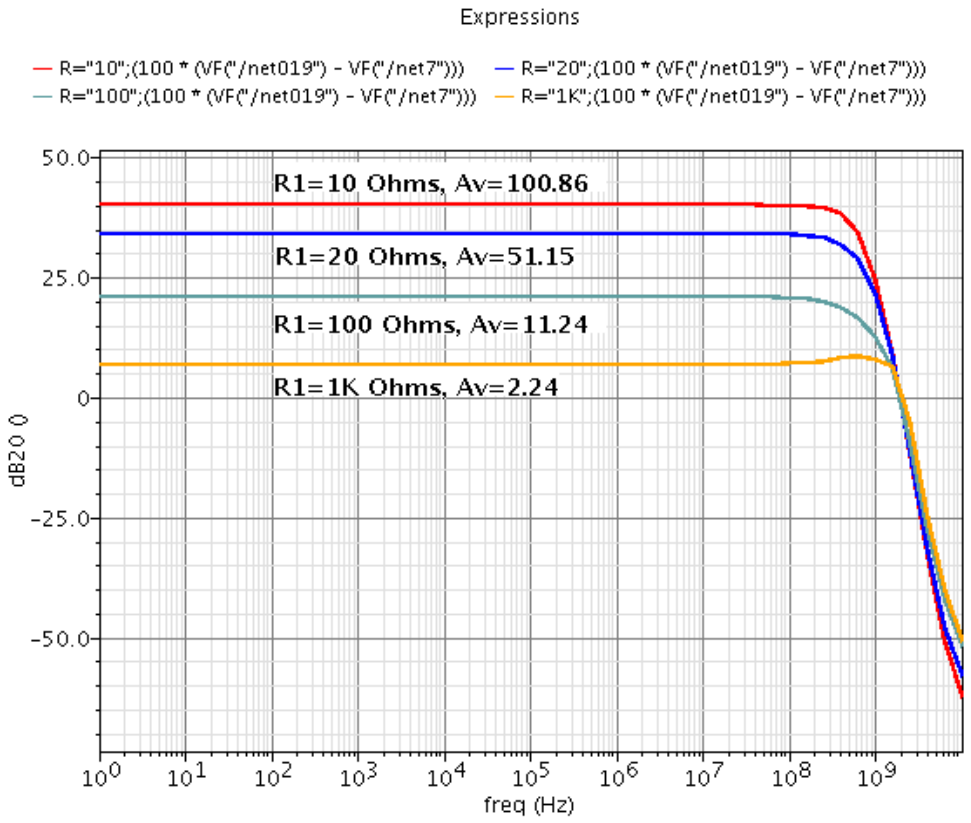


Figure 4-2: Magnitude frequency response of the fully differential voltage amplifier

4.2.2 Non-inverting voltage amplifier

If the input terminal Y_2 is grounded and the input signal (V_i) is applied at the other input terminal Y_1, the circuit becomes non-inverting voltage amplifier. The output is taken differentially across the output terminals W1 and W2 as shown in Figure 4-3.

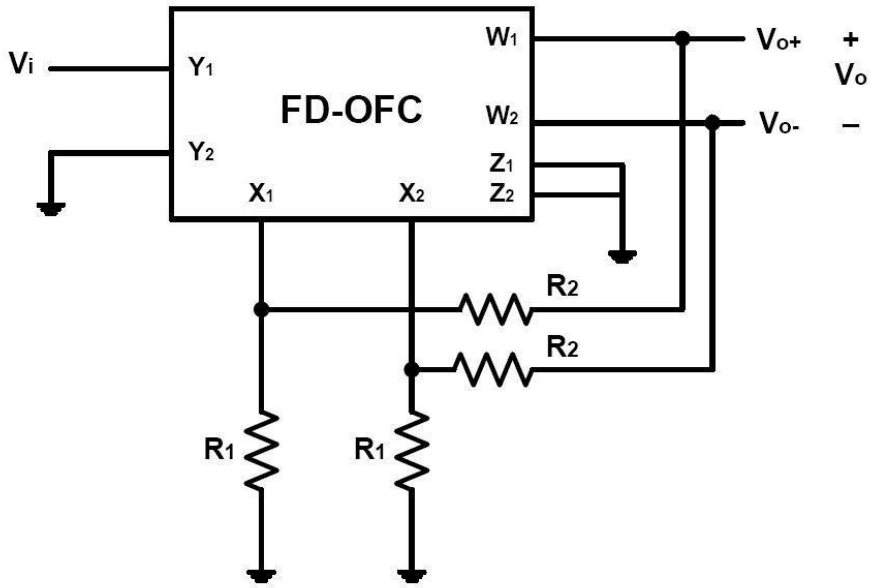


Figure 4-3: Non-inverting voltage amplifier

The voltage gain (A_v) is given by:

$$V_O = V_{O+} - V_{O-} = (V_i - 0)\left(1 + \frac{R_2}{R_1}\right) \quad (4\text{-}16)$$

$$A_V = \frac{V_O}{V_i} = 1 + \frac{R_2}{R_1} \quad (4\text{-}17)$$

4.2.3 Inverting voltage amplifier

If the input terminal Y_1 is grounded and the input signal (V_i) is applied at the other input terminal Y_2, the circuit becomes inverting voltage amplifier. The output is taken differentially across the output terminals W1 and W2 as shown in Figure 4-4.

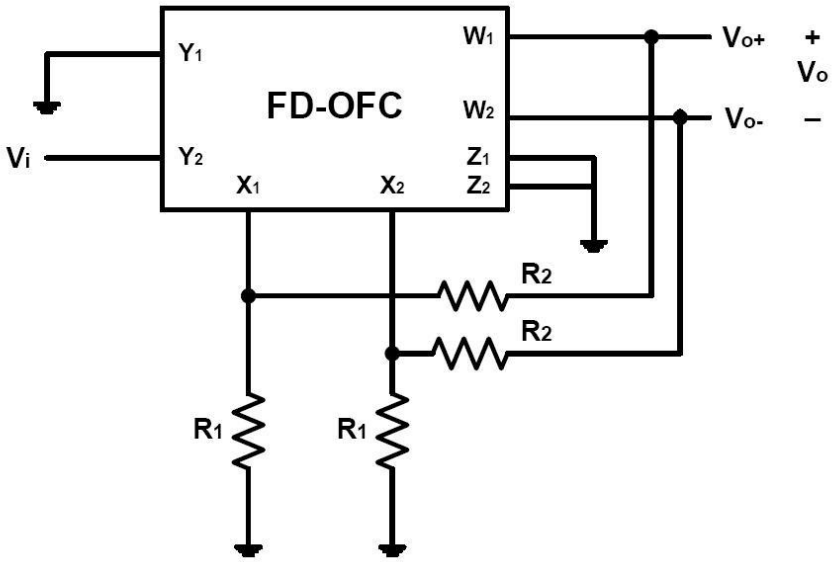


Figure 4-4: Inverting voltage amplifier

The voltage gain (A_v) is given by:

$$V_O = V_{O+} - V_{O-} = \left(0 - V_i\right)\left(1 + \frac{R_2}{R_1}\right) \tag{4-18}$$

$$A_V = \frac{V_O}{V_i} = -\left(1 + \frac{R_2}{R_1}\right) \tag{4-19}$$

4.3 Fully differential integrator

The FD-OFC can be used to implement the fully differential integrator as shown in Figure 4-5. The fully differential integrator is an important building block for applications like continuous time filters [17].The presented design is based on the same approach of the Operational Amplifier (Op-Amp) Miller's integrator [33] where: the node between the capacitor and resistance has zero voltage and the current flows through the capacitor and resistance is ideally the same. The input is applied differentially through two resistances which are connected to the input terminals X_1 and X_2. The output is taken differentially across the output terminals W1 and W2.

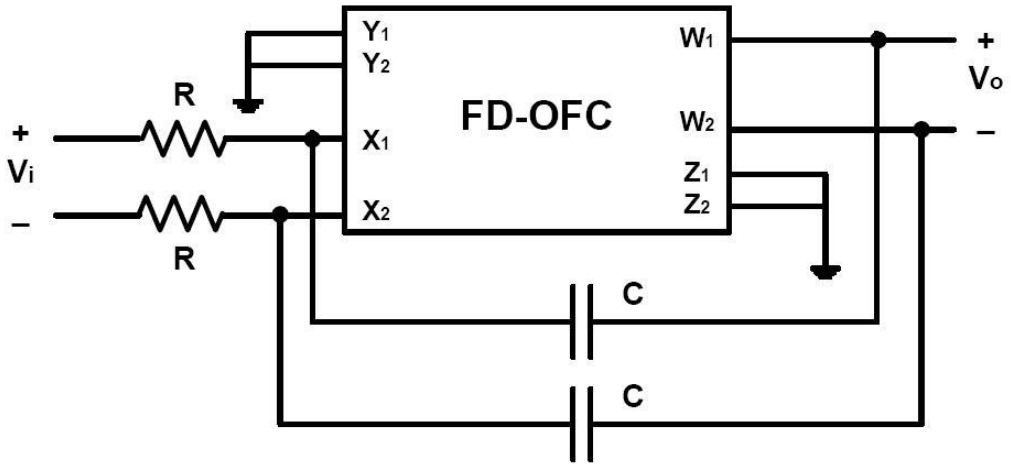


Figure 4-5: The fully differential integrator

The differential output (V_O) is given by:

$$V_O = \frac{-1}{SCR} V_i \tag{4-20}$$

The above expression can be derived as follows:

By applying KCL at terminal X1,

$$I_{X1} + \frac{V_{W1} - V_{X1}}{1/SC} = \frac{V_{X1} - V_{i+}}{R} \tag{4-21}$$

Substituting by

$$I_{X1} = \frac{V_{W1}}{Z_t(s)} \tag{4-22}$$

$$\because V_{X1} = V_{Y1} = 0 \quad \& \quad V_{W1} = V_{O+} \tag{4-23}$$

$$\frac{V_{O+}}{Z_t(s)} + \frac{V_{O+}}{1/SC} = \frac{-V_{i+}}{R_1} \tag{4-24}$$

$$V_{O+}\left(SC + \frac{1}{Z_t(s)}\right) = \frac{-V_{i+}}{R} \tag{4-25}$$

$$V_{O+} = V_{W1} = \frac{-V_{i+}}{R} \cdot \frac{1}{\left(SC + \frac{1}{Z_t(s)}\right)} \tag{4-26}$$

$$V_{O+} = V_{W1} = \frac{-V_{i+}}{SCR} \cdot \frac{1}{\left(1 + \frac{1}{SCZ_t(s)}\right)} \tag{4-27}$$

Similarly,

$$\because V_{X2} = V_{Y2} = 0 \quad \& \quad V_{W2} = V_{O-} \tag{4-28}$$

$$V_{O-} = V_{W2} = \frac{-V_{i-}}{SCR} \cdot \frac{1}{\left(1 + \frac{1}{SCZ_t(s)}\right)} \tag{4-29}$$

$$V_{O+} - V_{O-} = V_{W1} - V_{W2} = \frac{-\left(V_{i+} - V_{i-}\right)}{SCR} \cdot \frac{1}{\left(1 + \frac{1}{SCZ_t(s)}\right)} \tag{4-30}$$

$$V_O = \frac{-V_i}{SCR} \cdot \frac{1}{\left(1 + \frac{1}{SCZ_t(s)}\right)} \tag{4-31}$$

$$V_O = \frac{-V_i}{SCR} \cdot \varepsilon(s) \tag{4-32}$$

where ε(s) is the error function and can be expressed as:

$$\varepsilon(s) = \frac{1}{\left(1 + \frac{1}{SCZ_t(s)}\right)} \tag{4-33}$$

Ideally, the trans-impedance gain Zt(s) is considered very large (infinite) which leads to a unity error function (i.e. $\varepsilon(s) \approx 1$).

$$V_O = \frac{-1}{SCR} V_i \tag{4-34}$$

4.3.1 Circuit simulation

The fully differential integrator circuit is simulated using UMC 130 nm CMOS-based technology kit in Cadence environment. The entire circuit is simulated using the same transistor specification of the FD-OFC and 1.2 Volt biasing conditions.

The performance is verified by applying a square wave of 1Volt peak value and frequency of 100 KHz (T = 10 μs) as input signal. The passive component values are selected as follows, R = 10 KΩ and C = 250 pf. Both input and steady state output waveforms are shown in Figure 4-6 where the output is a triangular wave.

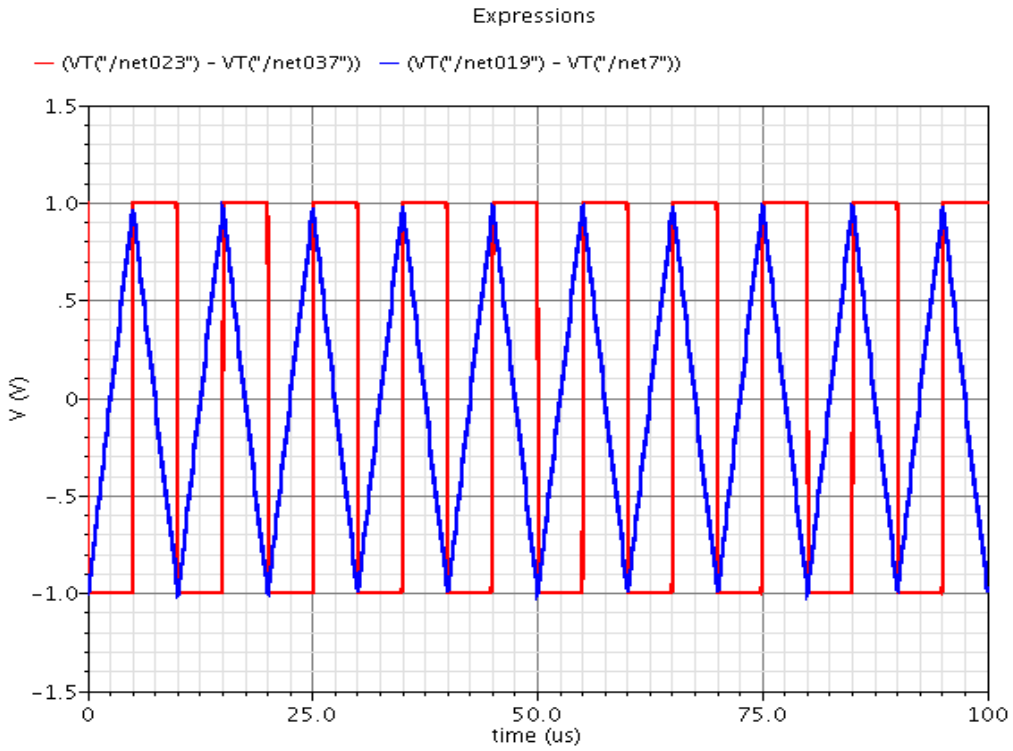


Figure 4-6: The fully differential integrator output along with the square wave input

4.4 Fully differential Current Conveyor (FDCCII+)

The FD-OFC can be configured as non-inverting Fully Differential second generation Current Conveyor (FDCCII+) as shown in Figure 4-7. This can be done similar to configuring the conventional OFC as non-inverting second generation Current conveyor (CCII+) [26,29]. The voltage following action occurs between the input terminals Y_1 and Y_2 to the other input terminals X_1 and X_2. The currents at the input terminals X_1 and X_2 are conveyed in phase to the output terminals Z_1 and Z_2.

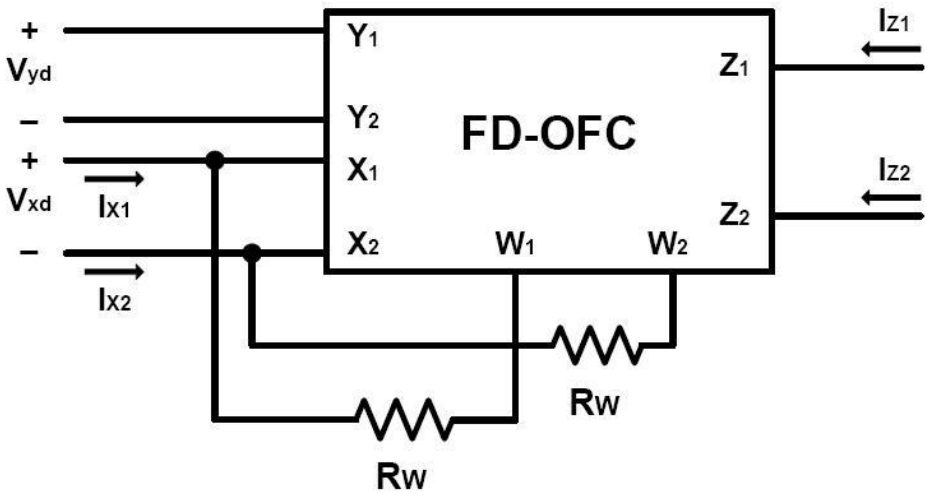


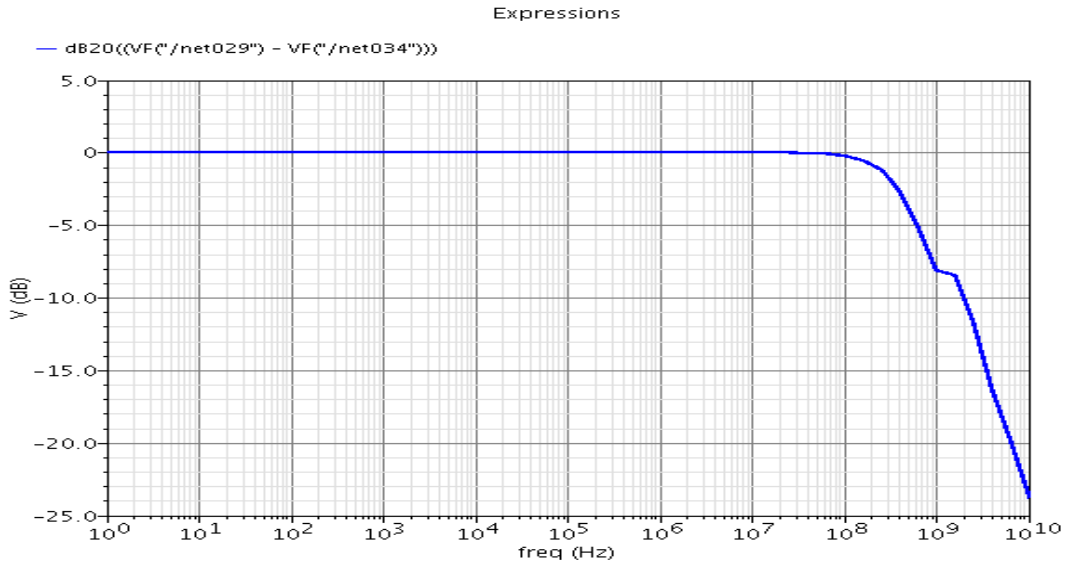
Figure 4-7: Non-inverting fully differential current conveyor (FDCCII+)

4.4.1 Circuit simulation

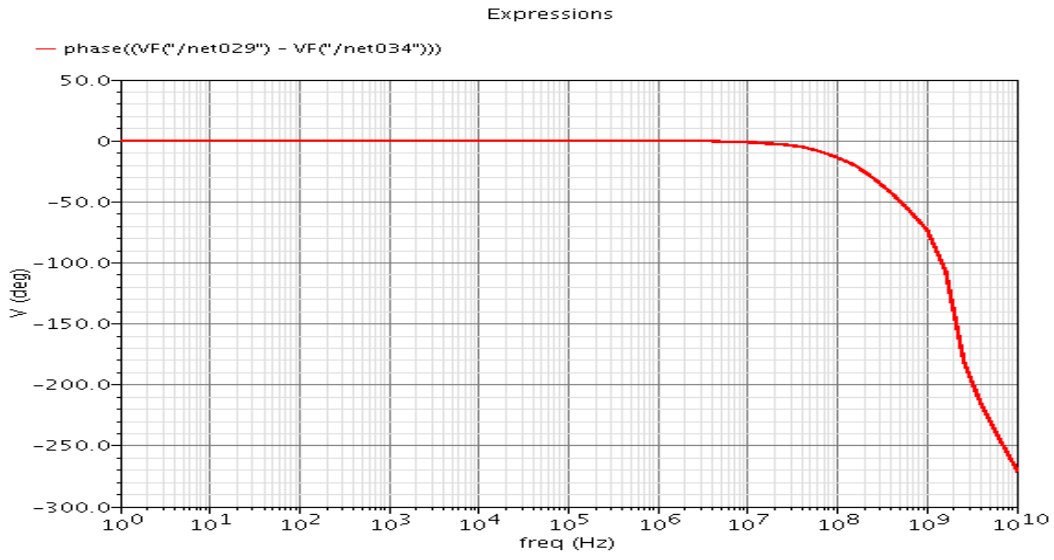
The fully differential integrator circuit is simulated using UMC 130 nm CMOS-based technology kit in Cadence environment. The entire circuit is simulated using the same transistor specification of the FD-OFC and 1.2 Volt biasing conditions. The FDCCII+ is simulated with R_w = 1 KΩ.

Figures 4-8 (a) & (b) show the AC characteristics between the X and Y terminals' differential Voltages (V_{xd} / V_{yd}). Figure 4-8(a) plots the magnitude frequency response between X and Y terminals' Voltages (in dB) while, Figure 4-8(b) plots the phase frequency response between X and Y terminals' voltages (in degrees).

Clearly these two figures confirm the voltage following action between the two terminals in the differential form as well as distortion-free transmission between the two terminals. The 3-dB frequency (Bandwidth) for open circuit voltage transfer gain is 400 MHz.



(a)



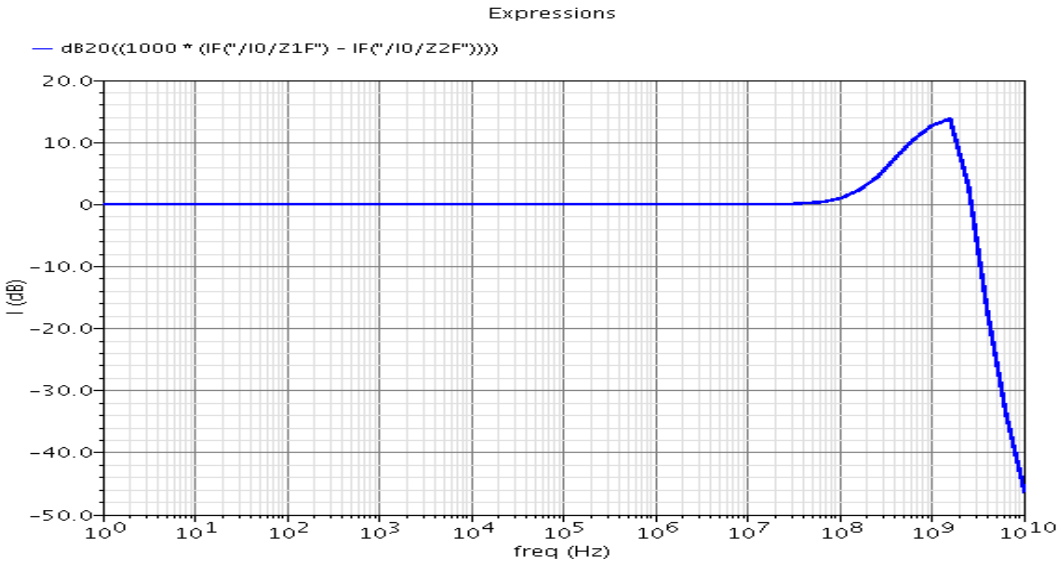
(b)

Figure 4-8: AC characteristics between X and Y terminals' voltages (Vxd / Vyd)

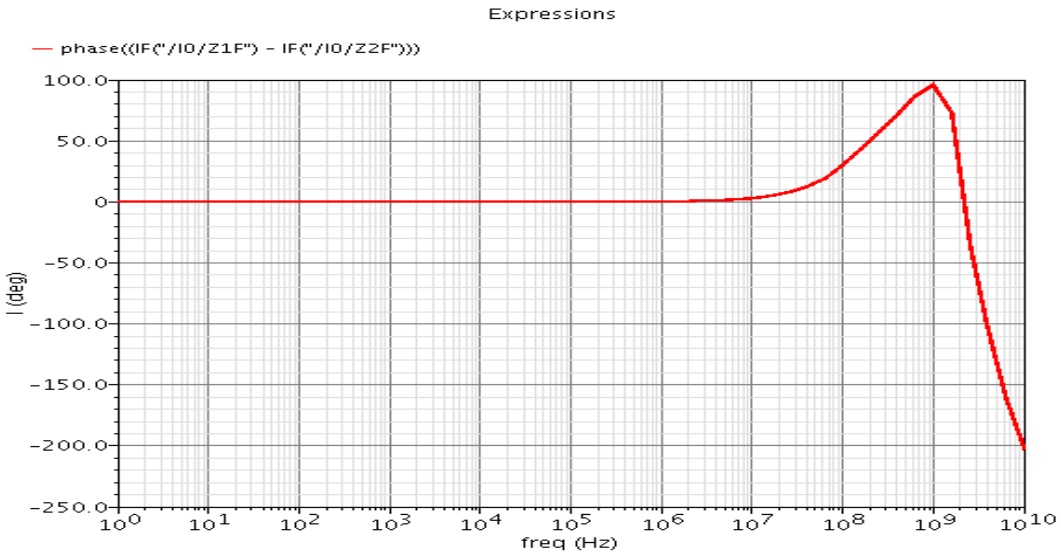
(a) Magnitude frequency response (b) Phase frequency response

Figures 4-9 (a) & (b) show the AC characteristics between the Z and X terminals' differential currents (I_{zd} / I_{xd}). Figure 4-9(a) plots the magnitude frequency

response between Z and X terminals' currents (in dB) while, Figure 3-9(b) plots the phase frequency response between Z and X terminals' currents (in degrees). These two figures confirm the validity of the current following action between the two terminals in the differential form. The current differential gain is invariant and equals one (0 dB) for AC signals having frequencies up to about 50 MHz. The phase shift between both terminals is zero for frequencies ranging from 0 to about 10 MHz.



(a)



(b)

Figure 4-9: AC characteristics between Z and X terminals' currents (Izd / Ixd)

(a) Magnitude frequency response (b) Phase frequency response

4.5 Current mode instrumentation amplifier (CMIA)

Instrumentation amplifiers are widely used in many application areas, such as: medical instrumentation [35,36], sensor readout integrated circuits [37] and data acquisition [1]. Instrumentation amplifiers are mainly used to reject the unwanted common mode signal/noise. The current mode instrumentation amplifiers have advantages over the voltage mode instrumentation amplifiers. For example, they don't require accurate resistor matching for high common mode rejection ratio (CMRR). Also, current mode instrumentation amplifiers have higher bandwidth which is independent on the gain. Most of the current mode instrumentation amplifiers are implemented using second generation Current Conveyors (CCII) or Operational Floating Conveyors (OFC) [39-46].

4.5.1 CMIA using two CCII+

The CMIA can be implemented using two non-inverting second generation Current Conveyers (CCII+) [39,44] as shown in Figure 4-10. The design contains also the gain setting resistance R_G and the load resistance R_L. Simplicity is the advantage of this design but the accuracy of the design is limited by the tolerance of terminal X equivalent input resistance R_X.

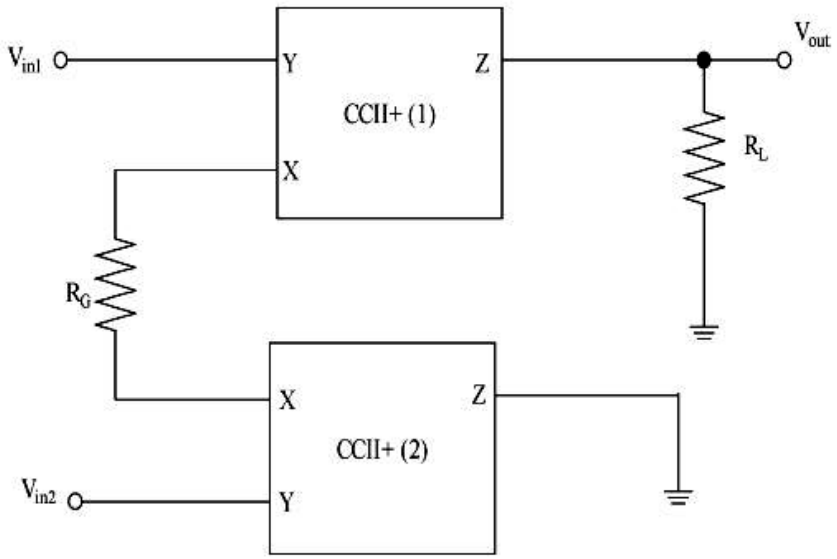


Figure 4-10: CMIA using two CCII+ [39,44]

The differential mode gain is $A_d(s)$ is given by:

$$A_d(S) = \frac{V_O}{V_{i1} - V_{i2}} = \frac{R_L}{R_G + 2R_X} \cdot \frac{1}{1 + SCR_L} \quad (4\text{-}35)$$

where C is the CCII+ equivalent output capacitance

4.5.2 CMIA using three CCII+

The CMIA can be implemented using three non-inverting second generation Current Conveyers (CCII+) [40,44] as shown in Figure 4-11. The design contains also the gain setting resistance R_G and the load resistance R_L. This design has higher gain and higher CMRR compared to the previous design but the accuracy of the design is still limited by the tolerance of terminal X equivalent input resistance R_X.

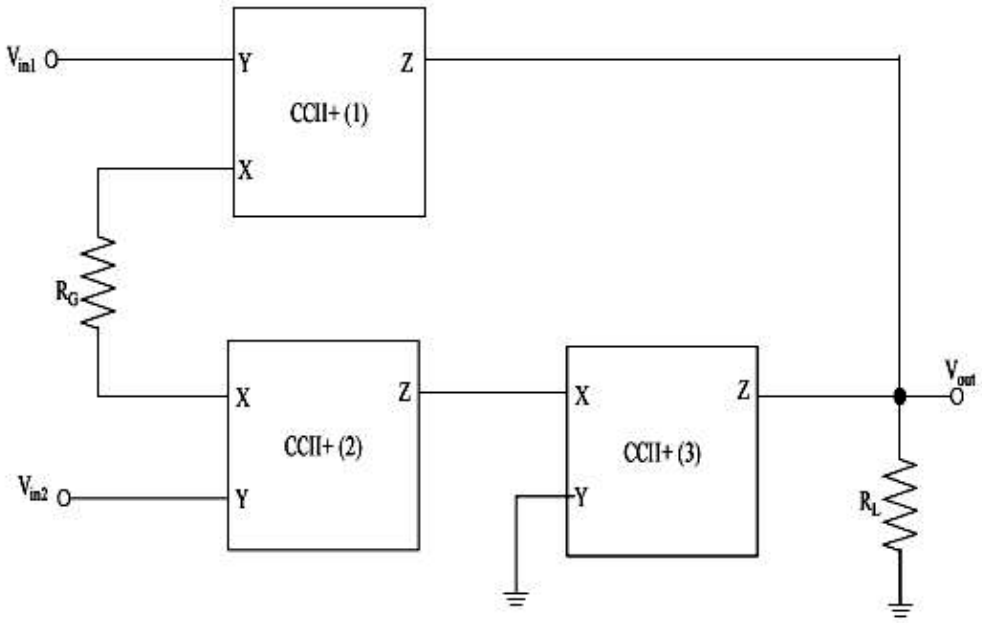


Figure 4-11: CMIA using three CCII+ [40,44]

The differential mode gain is $A_d(s)$ is given by:

$$A_d(S) = \frac{V_O}{V_{i1} - V_{i2}} = \frac{2R_L}{R_G + 2R_X} \cdot \frac{1}{1 + SCR_L} \quad (4\text{-}36)$$

where C is the CCII+ equivalent output capacitance

4.5.3 CMIA using two OFCC

As shown in Figure 4-12, two Operational Floating Current Conveyor (OFCC) can be used to implement the CMIA [32,44]. The design contains also the gain setting resistance R_G and the load resistance R_L in addition to two feedback resistances (R_{W1} and R_{W2}). These feedback resistances allows the OFCC to operate as CCII+ or CCII- while simultaneously reduces the input resistance of port X [,]. This design is more accurate than the two previous designs because it's independent on terminal X input resistance R_X and depends only on the external resistances R_G and R_L.

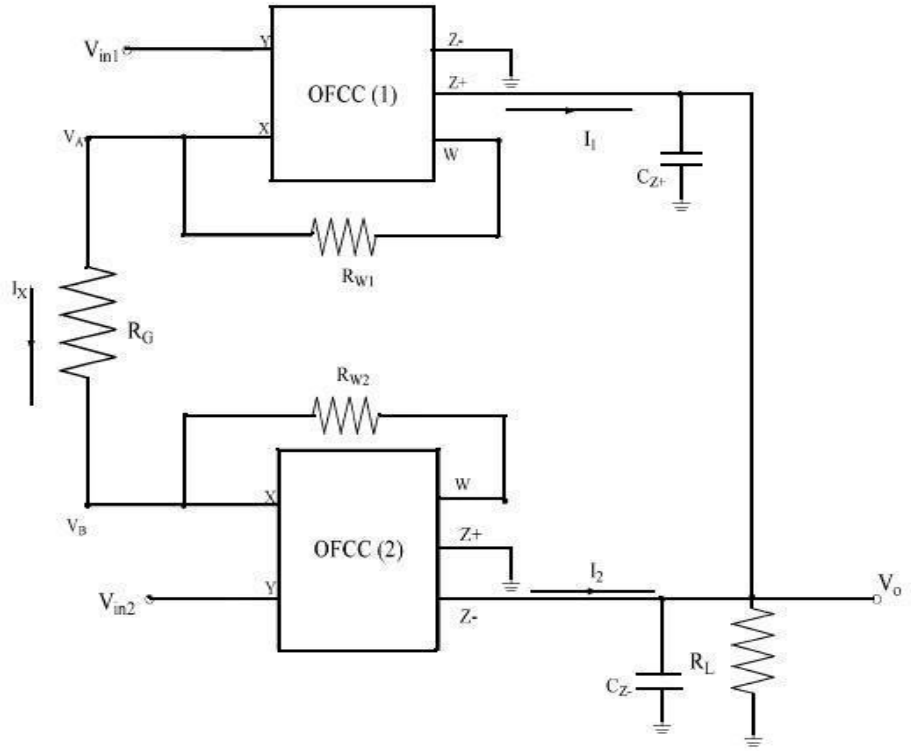


Figure 4-12: CMIA using two OFCC [32,44]

For ideal OFCC, the differential mode gain $A_d(s)$ can be derived as follows:

$$I_X = \frac{V_A - V_B}{R_G} = \frac{V_{in1} - V_{in2}}{R_G} \quad (4\text{-}37)$$

$$I_1 = I_X \quad \& \quad I_2 = I_X \quad (4\text{-}38)$$

$$V_O = (I_1 + I_2)\left(R_L \,//\, \frac{1}{SC_Z}\right) \tag{4-39}$$

where $C_Z = C_{Z1} + C_{Z2}$, is the equivalent capacitance of the output node

$$V_O = \frac{2(V_{in1} - V_{in2})}{R_G}\left(R_L \,//\, \frac{1}{SC_Z}\right) \tag{4-40}$$

$$V_O = \frac{2(V_{in1} - V_{in2})}{R_G}\left(\frac{R_L}{1 + SC_Z R_L}\right) \tag{4-41}$$

The differential mode gain is $A_d(s)$ can be is given by:

$$A_d(S) = \frac{V_O}{V_{in1} - V_{in2}} = \frac{2R_L}{R_G\left(1 + SC_Z R_L\right)} \tag{4-42}$$

It is clear from the above equation that the ratio $2R_L/R_G$ controls the differential gain while the bandwidth is set using $C_Z R_L$. This means that the differential gain can be controlled by R_G without affecting the bandwidth.

4.5.4 The proposed CMIA using one FD-OFC

Figure 4-13 shows the proposed CMIA using one Fully Differential Operational Floating Conveyor (FD-OFC). The design contains also the gain setting resistance R_G and the load resistance R_L in addition to two feedback resistances (R_{W1} and R_{W2}). These feedback resistances allows the FD-OFC to operate as CCII+ while simultaneously reduces the input resistance of port X similar to the conventional OFC [26,29]. This design is also more accurate than the first two designs because it's independent on terminal X input resistance R_X and depends only on the external resistances R_G and R_L. It gives less gain than the previous one (for the same resistance values) but it uses only one building block (FD-OFC) and provides higher bandwidth compared to the other designs.

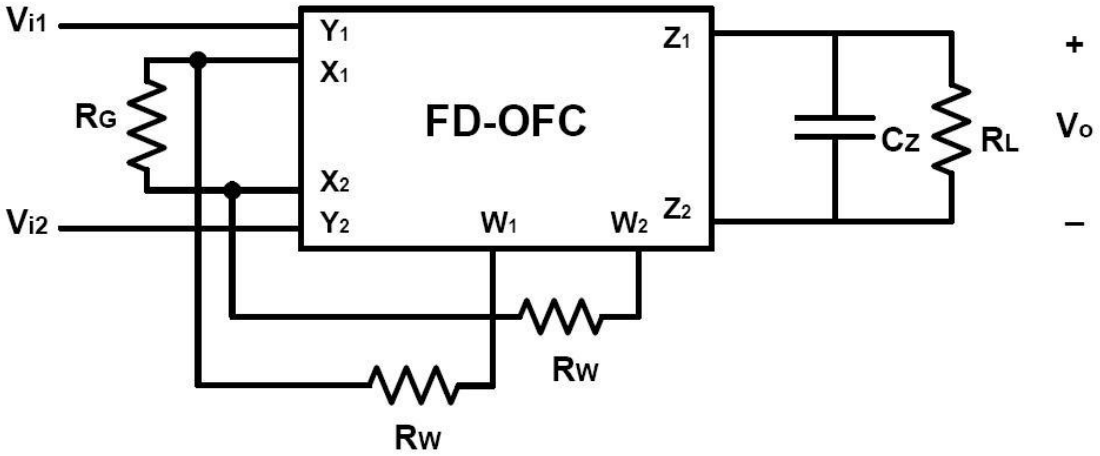


Figure 4-13: The proposed CMIA using one FD-OFC

Similar to the previous analysis, the differential mode gain $A_d(s)$ can be derived as follows:

$$I_X = \frac{V_A - V_B}{R_G} = \frac{V_{in1} - V_{in2}}{R_G} \tag{4-43}$$

$$I_L = I_X \tag{4-44}$$

$$V_O = I_X \left(R_L \,//\, \frac{1}{SC_Z} \right) \tag{4-45}$$

where C_Z is the equivalent capacitance of the output node

$$V_O = \frac{\left(V_{in1} - V_{in2}\right)}{R_G} \left(R_L \,//\, \frac{1}{SC_Z} \right) \tag{4-46}$$

$$V_O = \frac{\left(V_{in1} - V_{in2}\right)}{R_G} \left(\frac{R_L}{1 + SC_Z R_L} \right) \tag{4-47}$$

The differential mode gain is $A_d(s)$ can be is given by:

$$A_d(S) = \frac{V_O}{V_{in1} - V_{in2}} = \frac{R_L}{R_G \left(1 + SC_Z R_L\right)} \tag{4-48}$$

It is clear from the above equation that the ratio R_L/R_G controls the differential gain while the bandwidth is set using $C_Z R_L$. This means that the differential gain can be controlled by R_G without affecting the bandwidth.

4.5.5 Simulation results of the proposed CMIA

The CMIA using one FD-OFC circuit is simulated using UMC 130 nm CMOS-based technology kit in Cadence environment. The entire circuit is simulated using the same transistor specification of the FD-OFC and 1.2 Volt biasing conditions.

The frequency response of different differential gains of the circuit are shown in Figure 4-14 using R_W = 0.25 KΩ, R_L = 1 KΩ and R_G = 10 Ω, 20 Ω, 50 Ω and 100 Ω. The actual differential gain is much closer to the ideal gain for smaller gain values. These different gain values are invariant for AC signals having frequencies up to about 100 MHz. The differential gain bandwidth is approximately gain independent (it varies between 630 MHz and 975 MHz for the shown differential gain values). The Common Mode Rejection Ratio (CMRR) is measured for the proposed CMIA for the different differential gain values [38]. As expected, using the FD-OFC as a fully differential building block led to a very high CMRR.

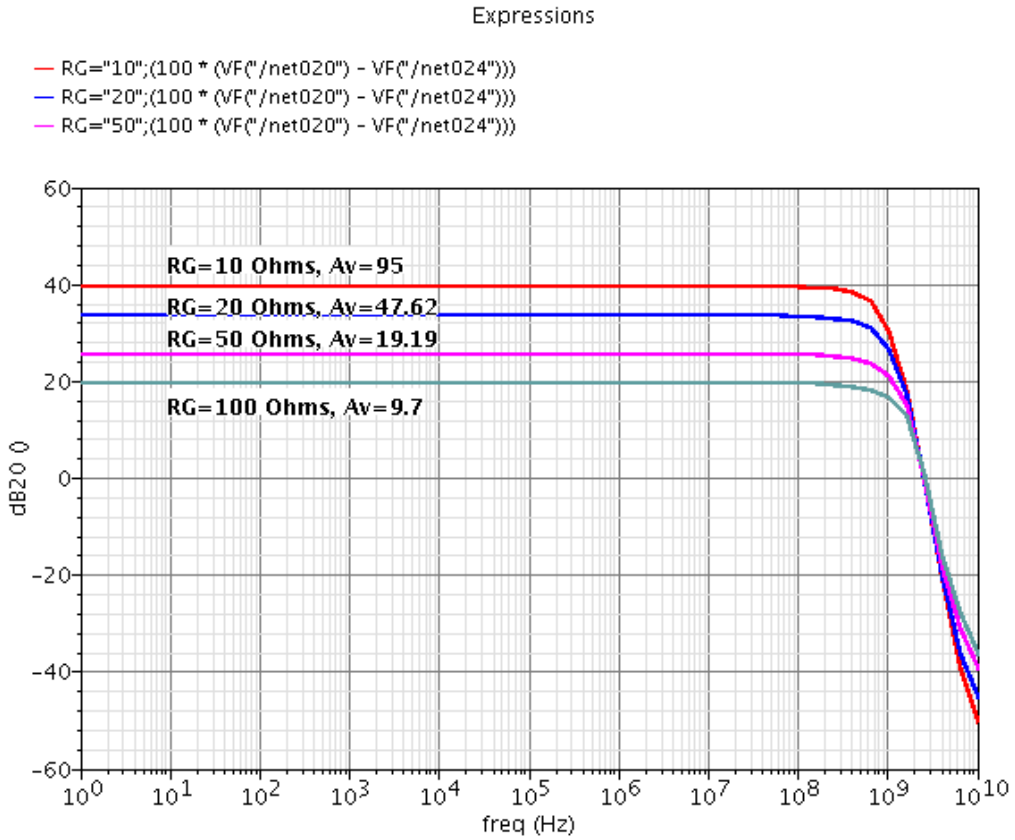


Figure 4-14: Magnitude frequency response of the proposed CMIA

4.5.6 Comparison between the proposed CMIA and other designs

The proposed CMIA exhibits wider bandwidth compared to other designs, higher CMRR and uses only one building block (FD-OFC). Table 4-1 shows a comparison between the proposed CMIA and other conveyor designs based on the comparisons conducted in [44,46].

Ref. No.	Differential Gain (dB)	Diff. Gain -3dB Freq.	CMRR (dB)	CMRR -3dB Freq.	Building Blocks
[39]	20, 26, 29.54, 32	1.2-2.3 MHz	100	NA	2 CCII+
[40]	40, 25, 5.7	1.44 MHz	95	65 KHz	3 CCII+
[41]	29, 24, 19	591.6 KHz	95	2 KHz	2 CCII+
[42]	40, 20, 0	1.5-2.97 KHz	55	10 KHz	2 CCII+, 2 Op-Amp
[43]	14, 19.6, 25	10 MHz	147	35 KHz	3 CCCII
[44]	32, 26, 12, 6	1.2 MHz	76	185 KHz	2 OFCC
[32]	32, 26, 12, 6	32.7 MHz	61	292 MHz	2 OFCC
[45]	16.7, 21, 25.4, 28.7	70.1 MHz	142	NA	2 CCCII
[46] Des. 3	21, 25, 31, 36	20.85 MHz	55	349 KHz	3 OFCC
[46] Des. 7	23, 17, 11, 9	30 MHz	85	32 KHz	4 OFCC
Proposed	39.55, 33.6, 25.7, 19.74	630 MHz - 975 MHz	243	104 MHz	1 FD-OFC

Table 4-1: Comparison between different designs of the CMIA

Chapter 5: Conclusion and Future Work

5.1 Conclusion

A novel concept of the Fully Differential Operational Floating Conveyor (FD-OFC) is presented in this thesis. The FD-OFC as a novel general purpose analog building block is an extension of the conventional Operational Floating Conveyor (OFC). The FD-OFC is a member of the analog signal processing circuits that are operating in the current mode. This means that the proposed device has the fundamental advantage of independent gain and bandwidth.

A CMOS-based circuit designs for the proposed device are introduced and simulated. Two different designs/realizations are implemented and a comparison is made between these two realizations. The second realization consumes less power and achieves higher DC open loop trans-impedance gain. Simulation results indicate that the proposed concept and circuit designs are perfectly suitable for low power, high speed applications as circuits can operate under biasing conditions as low as 1.2 Volts and a bandwidth as high as 600 MHz. Moreover, the fully differential action offered by the proposed device makes it a perfect candidate for applications in which a high noise rejection ratio is desired.

Different FD-OFC based applications are presented and simulated. These applications are fully differential voltage amplifier, Non-inverting voltage amplifier, Inverting voltage amplifier, fully differential integrator, fully differential second generation current conveyor (FDCCII) and current mode instrumentation amplifier (CMIA). Simulation results verified the high performance along with the extended bandwidth of these applications.

5.2 Future work

The presented concept and work in this thesis can be extended and used for future work as follows:

- More applications will be implemented and simulated using the FD-OFC such as different types of amplifiers, oscillators and active filters.
- The layout of the FD-OFC will be developed to achieve the minimum possible area.
- The device will be fabricated using the 130 nm CMOS technology.
- The experimental results will be compared with the simulation results.
- Compensation techniques can be tested to enhance the device performance.
- The device can be simulated and fabricated using different technology sizes like 65 nm to study the effect of scaling on device performance.
- Process variations can be studied for the fabricated device.

List of Publications

Accepted and published papers

Elgemmazy, H., A. Helmy, H. Mostafa, and Y. Ismail, "A Novel CMOS-based Fully Differential Operational Floating Conveyor", IEEE International Symposium on Very Large Scale Integration (ISVLSI 2017), Bochum-Germany, pp. 604-608, 2017.

Submitted papers (under review)

Elgemmazy, H., A. Helmy, H. Mostafa, and Y. Ismail, "An Improved Design for High Speed Analog Applications of The Fully differential Operational Floating Conveyor".

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