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On the production testing of analog and digital circuits

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ON THE PRODUCTION TESTING OF ANALOG AND DIGITAL CIRCUITS

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To my Family and Friends

Abstract

This thesis focuses on the production testing of Analog and Digital circuits. First, it addresses the issue of finding a high coverage minimum test set for the second generation current conveyor as this was not tackled before. The circuit under test is used in active capacitance multipliers, V-I scalar circuits, Biquadratic filters and many other applications. This circuit is often used to implement voltage followers, current followers and voltage to current converters. Five faults are assumed per transistor. It is shown that, to obtain 100% fault coverage, the CCII has to be operated in voltage to current converter mode. Only two test values are required to obtain this fault coverage. Additionally, the thesis focuses on the production testing of Memristor Ratioed Logic (MRL) gates because this was not studied before. MRL is a family that uses memristors along with CMOS inverters to design logic gates. Two-input NAND and NOR gates are investigated using the stuck at fault model for the memristors and the five-fault model for the transistors. It is shown that in order to obtain full coverage for the MRL NAND and NOR gates, two solutions are proposed. The first is the usage of scaled input voltages to prevent the output from falling in the undefined region. The second proposed solution is changing the switching threshold V_M of the CMOS inverter. In addition, it is shown that test speed and order should be taken into consideration. It is proven that three ordered test vectors are needed for full coverage in MRL NAND and NOR gates, which is different from the 100% coverage test set in the conventional NAND and NOR CMOS designs.

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List of Abbreviations

CMOS – Complementary Metal Oxide Semiconductor

VLSI – Very Large Scale Integration

OpAmp – Operational Amplifier

OTA – Operational Transconductance Amplifier

ADC's – Analog-Digital Converters

DAC's – Digital-Analog Converters

PLL – Phased Lock Loop

CCII – Second Generation Current Conveyor

CPL – Complementary Pass-Transistor Logic

MRL – Memristor Ratioed Logic

IC – Integrated Circuit

SAF – Stuck-at Fault

SOP – Stuck Open

SON – Stuck On

MTS – Minimum Test Set

CUT – Circuit Under Test

CCs – Current Conveyors

HP – Hewlett Packard

TEAM – ThrEshold Adaptive Memristor

Chapter 1
Introduction

1.1 Background

Advances in the microelectronics fabrication of Complementary Metal Oxide Semiconductor (CMOS) technology has allowed for increased level of integration of transistors per unit area and helped in reducing the cost of the chip. Due to CMOS technology scaling, more circuits could be integrated on a single chip. This increased design complexity created several challenges in many areas, one of which is manufacture test. Manufacture test is also known as Production testing. The manufacturing process for Very Large Scale Integration (VLSI) circuits is not perfect. So, because of different reasons, physical defects are introduced in the VLSI circuits. Therefore, manufacturing test is of great importance. Production testing ensures that a manufactured chip is functioning as expected. The main goal of the production testing is to identify all chips that do not function as expected due to defects. It is demanded that the production test be cost/time effective and it must cover as many defects as possible.

1.2 Contribution of this Thesis

Different Analog circuits such as operational amplifiers (Opamps), Operational Transconductance Amplifiers (OTAs), Analog-Digital Converters (ADC's) and Digital-Analog Converters (DAC's) and Phased Locked Loop (PLL) have been tested using different analog testing techniques. In this dissertation, we perform testing on another versatile current mode analog building block, namely the Second Generation Current Conveyor (CCII) using DC Testing (one of the analog testing techniques). The main target is to obtain the highest possible fault coverage and reduce the test cost/time. CCII was introduced in [1, 2]. It is used to implement voltage followers, current followers, voltage-current converters, integrators and differentiators. We utilize the fact that the CCII could be used to implement voltage-current converters to achieve the highest possible fault coverage and test the circuit efficiently.

Testing of digital circuits is well established compared to analog circuits. Digital circuits are often tested using the stuck-at fault model. However, using this fault model does not detect some physical defects. So the transistor level fault models are used to detect all possible defects. It is shown in the literature that testing CMOS, Complementary Pass Transistor Logic (CPL) and Dynamic Logic gates depends on the sequence of applying test vectors and the speed of their application. Usually, digital circuits are designed using transistors. However, due to limitations of technology scaling, a new emerging device called the memristor could be used to design logic gates. Memristors were theoretically predicted in 1971 by Chua [3]. Memristor Ratioed Logic (MRL) family uses memristors in conjunction with standard CMOS inverters to design logic gates. In this dissertation, we perform testing on the two-input NAND and NOR gates designed using MRL family. Testing MRL gates is challenging as some of the faults in the memristors cause the input of the inverter to fall in the undefined region and this might lead to test escapes. Therefore, we propose two different solutions to solve this problem. The first is to apply scaled input voltages to the input terminals. The second proposed solution is to design the CMOS inverter for testability by altering its switching threshold (V_M) to guarantee full coverage. In addition, the test sequence and speed is considered.

1.3 Thesis Organization

Chapter 2 explains the concept of production testing and why it is needed. Followed by that, the chapter explains the concept of fault modeling. It shows different fault models used at different levels of abstraction, along with the pros and cons of using these fault models. By the end of the chapter, testing of different analog circuits using different testing techniques is presented. Finally, various aspects in testing digital circuits are elaborated.

Chapter 3 discusses the testing of the CCII. It presents the results of testing the CCII under three different modes; voltage follower, current follower and voltage-current converter. These results are discussed, analyzed and explained within the chapter.

In Chapter 4, a brief overview about the memristors and MRL Family is given. Followed by that testing of two-input NAND and NOR gates results and discussion is provided.

Chapter 5 concludes the dissertation.

In Chapter 2, previous work done in the field of testing analog and digital circuits is shown. This mainly includes the description of different fault models that are used to represent the physical defects. In addition, different aspects in the testing of analog and digital circuits are elaborated.

Chapter 2
Fault Modeling and Testing of Analog and Digital Circuits

This chapter starts by explaining the concept of production testing and why it is important. Followed by that, important terms such as failure, fault and error are defined. In addition, fault models at different levels of abstraction are listed. Advantages and disadvantages of using fault models at different levels of abstraction are elaborated. Towards the end of this chapter, testing of different analog building blocks using different techniques is presented. Finally, testing digital circuits using different fault models is shown.

2.1 What is Production Testing and why it is important

A manufactured Integrated Circuit (IC) may not work properly, despite having a correct design. This can happen due to several reasons such as problems in the manufacturing process or during shipping [4, 5]. It is of great importance that any failure that can affect the functionality or the performance of the component be discovered early. Once a part is placed in a larger system or shipped to the customers, it becomes very expensive to discover it is malfunctioning. Production test is applied to the produced devices to make sure they meet the specification. Huge numbers of devices are produced every day; therefore testing each device must be cost-effective. Yet, the tests must also be accurate. In production tests, there usually are no fault diagnosis tests as in [6], i.e., the location of the fault is not important, and it is only functional go/no go test [7].

2.2 Faults and Fault Modeling

Faulty behavior in a circuit can be due to many factors. Some of these defects are introduced in the fabrication process or the fabrication material.

In order to introduce the concept of fault modeling, it is important to identify

some key terms that might be confused together. These terms are failure, fault and error.

A) Failure: It is sometimes referred to as a defect. A failure or defect in an electronic system is the unintended difference between the implemented hardware and its intended design.

B) Fault: A representation of a "defect" at the abstracted function level is called a fault. The difference between a defect and a fault is rather subtle. They are the imperfections in the hardware and function, respectively [7].

C) Error: A wrong output signal produced by a defective system is called an error. An error is an "effect" whose cause is some "defect."[7]

In order to mimic or represent the defect, fault modeling is needed. Figure 2.1 shows an example of a physical defect that is fault modeled. Several fault models are described in the following subsection.

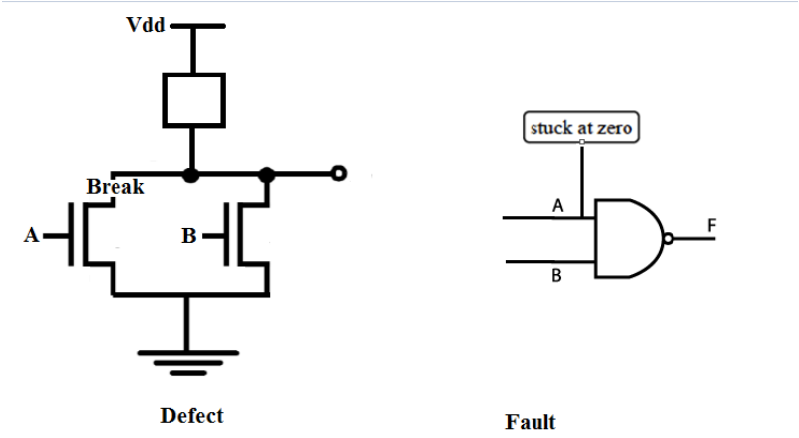

Figure 2.1: Physical Defect and its Fault Model

It should be noted that faults are of two types, catastrophic and parametric. Catastrophic faults are also known as hard faults; they cause a functional failure, i.e., wrong output. Parametric faults are also known as soft faults; they affect the characteristics of the manufactured circuit, i.e., delay constraints are not met for example. Catastrophic faults often occur due to manufacturing defects and parametric faults occur due to imperfections in IC manufacturing such as variations in the

threshold voltage of the transistors [7, 8].

2.2.1 Fault Models

Faults can be classified according to their level of abstraction. Figure 2.2 shows the different levels of abstraction that fault models can represent. A fault model is good if by testing the modeled faults, all physical defects are covered. The advantage of using fault models developed for lower level of abstraction is that they give a better representation of the actual physical failures that occur in the circuit, yet this also has the disadvantage of having a large number of possible faults that need to be considered in the fault list [7, 9]. In order to reduce the number of faults to be considered in the design, a good way is to go up in the design hierarchy and choose fault models that are at a higher abstraction level. This gives less number of faults since one fault at higher levels model several faults at lower levels. On the other hand, high level fault models cannot detect many faults that might be present in the lower abstraction level as will be shown later in the chapter.

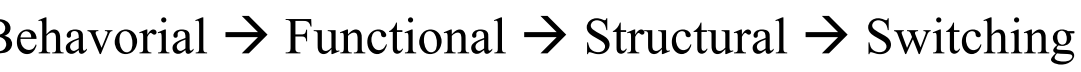

Figure 2.2: Classification of fault models according to their level of abstraction

The first abstraction level is the Behavioral level fault model, also known as RTL level fault model. These types of faults are defined at the highest level of abstraction. They are associated with failure modes of the constructs in hardware descriptive languages such as VHDL or Verilog [9]. Usually, the details of the design are unknown as the functions of the modules are expressed in programming constructs. As we go higher in the abstraction level, it becomes more and more difficult to find a direct link or a co-relation between a physical fault and a modeled fault. Many of the behavioral fault models can be mapped to actual physical failures in the chip. The derived test sets from such fault models were found to detect up to 85% of the faults belonging to fault models at lower levels like stuck-at faults for instance [9].

The second abstraction level is the functional level fault model. These are faults defined on the functional block level. They aim at ensuring that the functional block performs its expected functional and no other unintended functions are performed.

The third abstraction level is the Structural level fault Model, also known as logic/gate level fault models. These fault models are used to verify if the interconnections in a given circuit are functioning properly and can carry both logic 0 and 1 [7]. The most well-known and commonly used structural fault model is the stuck-at fault model. The stuck-at fault model (SAF) is described as follows:

Stuck-at Fault Model: A node is considered stuck-at-0 (s-a-0), if it always carries a logic '0' regardless of the value the node should have. Similarly, a node is stuck-at-1 (s-a-1) if it always carries logic '1' regardless of the value the node should have. They can model breaks in connection between transistors as shown above in Fig. 2.1. If the SAF is assumed to occur on only one line/node in the circuit, it is said to be a single SAF. Otherwise, if the SAF is assumed to occur on multiple lines/nodes simultaneously, it is said to be a multiple SAF. In a circuit of k interconnections/nodes, there are only $2k$ possible single stuck at faults while there are $3^k - 1$ multiple stuck at faults. Consequently, Multiple SAF is much more complex to find the minimum test for. This is why single SAF assumption is made to reduce the complexity of the test pattern generation. This is a good approximation due to the fact that a good stuck-at minimum test set that can detect all or almost all single SAF will most probably also detect all or almost all multiple SAF [10]. The Stuck-at fault model is the most widely used fault model in the industry. This goes back to its straight forward test generation techniques, the fact that it can be applied to various semiconductor technologies, and most importantly its high coverage of physical defects.

The Fourth abstraction level is the switching level fault Model, also known as transistor level fault model as faults are defined at the transistor level. They give more accurate representation of the actual physical failures that occur in the circuit since it is the closest to the physical layer. On the other hand, they are much complex than higher level models since they include the maximum number of faults as faults are modeled on

each transistor in a given gate. There are several transistor level fault models in the literature as shown below.

Stuck-Open and Stuck-On Fault Model: In [11], the transistor is considered as an ideal switch; a defect may cause the transistor to either be on or off. A transistor is said to be stuck-open (SOP) if it is always OFF regardless of its gate voltage; this also known as the non-conducting state. Similarly, A transistor is said to be stuck-on (SON) if it is always ON regardless of its gate voltage; this also known as the conducting state.

Two-Fault Model: In [12], two faults per transistor are considered. A resistive open fault modeled by R_{open} series resistance between the drain and the rest of the circuitry. A resistive short fault modeled by R_{short} between the drain and source of the MOS transistor. This fault model is shown in Fig. 2.3a.

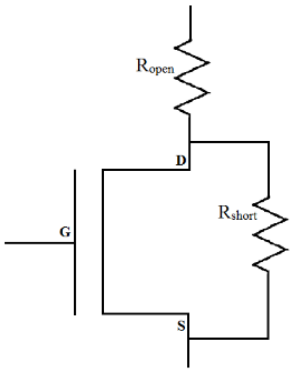

Figure 2.3a: Two-Fault Model

Six-Fault Model: The six-fault model includes six faults per transistor. These faults are as follows:

- Gate-Source short circuited
- Gate-Drain short circuited
- Drain-Source short circuited
- Source open circuited
- Drain open circuited
- Gate open circuited

This fault model was proposed in [13] and is shown in Fig. 2.3b. However, researchers do not use this model frequently because of the open gate fault. This fault is not included

as it is difficult to model or simulate with any degree of confidence. Therefore, the five-fault model is used as explained below.

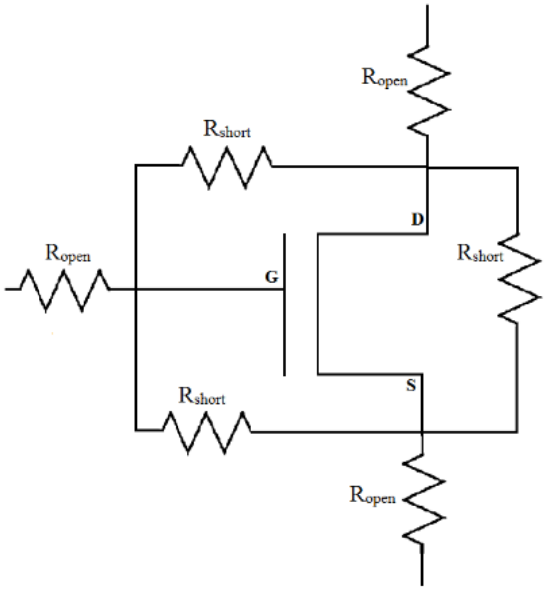

Figure 2.3b: Six-Fault Model

Five-Fault Model: The five-fault model proposed in [14] includes five faults per transistor. These faults are as follows:

- Gate-Source short circuited
- Gate-Drain short circuited
- Drain-Source short circuited
- Source open circuited
- Drain open circuited

A resistive open circuit fault is modeled by inserting R_{open} resistance at the MOS terminal that is open circuited. A resistive short circuit fault is modeled by connecting R_{short} resistance between the two MOS terminals that are short circuited. This fault model is shown in Fig. 2.3c.

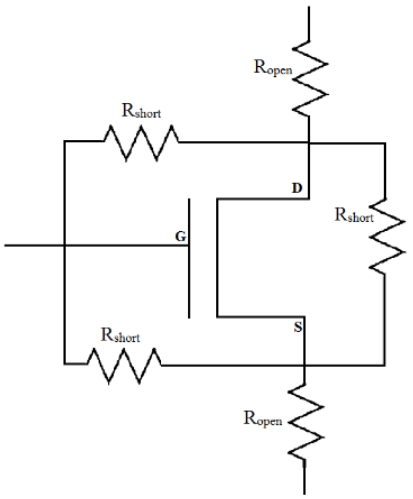

Figure 2.3c: Five-Fault Model

2.3 Testing Analog Circuits

Electronic circuits are mainly divided into two main subdivisions, Analog and Digital circuits. Testing digital circuits is well established in comparison to their analog counterparts. In this section, different analog testing techniques used in the literature are presented.

The first technique is known as AC Testing. In [15], testing of the operational amplifier (opamp) is studied. The five-fault model is used and faults are injected one at a time. R_{open} is taken to be 10MΩ and R_{short} is taken to be 1Ω. Out of 35 faults (21 R_{short} and 14 R_{open}) one fault is removed from the fault list because this fault does not affect the functionality of the circuit. This fault is the Gate-Source short circuit of the PMOS transistor used to design the current mirror. Hence the fault list includes a total of 34 faults. Out of the 34 faults, 31 faults are detected using the input vector 1KHz frequency and 100mV amplitude to the inverting input of the opamp. The fault is detected if there is a 300mV deviation or more when compared to the output of the fault-free scenario. This produces fault coverage of 91.2%. In order to increase the fault coverage, [15] proposes another technique known as power supply voltage control; it is also known as supply voltage variation. In this method, the supply voltage V_{dd} is swept from 0V to 5V. The three undetected faults were detected when the supply voltage varied from 66mV to

366mV. Using this technique, full fault coverage is obtained. The main idea behind this technique is to force the transistors to work in different operation regions as compared to the operation region they should be working in during the fault free situation.

In [16], the power supply voltage control technique was used for a bigger circuit, namely a Phased Locked Loop (PLL) to validate that this technique is of good use. However, open faults were not considered; only resistive shorts were investigated.

Another technique of testing analog circuits is by providing an AC power supply voltage instead of the traditional DC power supply V_{dd}. In [17], catastrophic faults were detected by AC power supply voltage at high frequency (10MHz).

All the circuits under test discussed above are voltage mode circuits. Another approach to design circuits is current mode. The main advantage of current mode circuits is that they operate high frequencies. In addition, they are power efficient.

In [18], Operational Transconductance Amplifier (current mode circuit) is tested for catastrophic faults. The 180nm CMOS technology was used and the five-fault model was considered in the study. Faults were assumed one at a time. The input voltage is swept from V_{SS} to V_{DD} and the output is tracked. The fault is considered detected if the output has a deviation of 10% from the fault-free output. It was found that two test values are needed V_{SS} and V_{DD} are needed to obtain 93.3% fault coverage.

In [19], the same OTA is tested for catastrophic faults. The 90nm CMOS technology is used. The six-fault model was assumed. The faults were inserted one at a time. In order to reduce test time and consequently test cost, the minimum number of test values is found that would produce the highest possible fault coverage. The testing technique used in this study is known as DC Testing. The input voltage is swept from V_{SS} to V_{DD} and the output is tracked. The fault is detected if there is deviation of more than 10% compared to the fault-free output [14]. R_{open} was modeled by 100MΩ and R_{short} is modeled by 10Ω. It was found that two test values were able to detect 34 faults of 36 faults considered in the fault list, yielding 94.4% fault coverage. In addition, the effect of a change in the value of the resistive short fault between any two transistor terminals is studied using Monte Carlo analysis. R_{short} value was varied from 10Ω to 1KΩ. It was shown that the coverage is independent of the value of this resistance.

2.4 Testing Digital Circuits

Testing digital circuits is well established as compared to their analog counterparts. The most commonly used fault model in the industry is the stuck-at fault model. As mentioned earlier, this is a gate/structural level fault model. One of its advantages is that the number of faults to be considered is lower than the number of faults in the fault list when using a transistor level fault model. It was found by many researchers [11, 20, 21], that one of the disadvantages of using the stuck-at fault model is that it suffers some test escapes as elaborated below.

Table 2.1 shows the test results of the two input NAND gate using the stuck-at fault model. A and B are the inputs, Y is the fault-free output. The fault A stuck-at '0' is denoted by A s-a-0. When this fault (A s-a-0) occurs the output will always be logic high. This shows that this fault is only detected by the input vector AB=11 because the output logic is different from the fault-free output logic. The task done in Table 2.1 is known as test pattern generation. These patterns need to be minimized in order to test the circuit in a small amount of time. We can realize that the fault Y s-a-1 is detected by three vectors 00, 01 and 10. The vector 00 is redundant because the same fault could be detected using two other vectors that will detect other faults. Therefore 00 is not needed to test two-input NAND gate. Hence, the minimum test set (MTS) is {01, 10 and 11}.

Table 2.1: Testing Two-input NAND Gate using the Stuck-at Fault Model

A	B	Y	A s-a-0	A s-a-1	B s-a-0	B s-a-1	Y s-a-0	Y s-a-1
0	0	1	1	1	1	1	0	1
0	1	1	1	0	1	1	0	1
1	0	1	1	1	1	0	0	1
1	1	0	1	0	1	0	0	1

In [11, 20, 21], the transistor level fault model was used to test the conventional CMOS two-input NAND gate design shown in Fig. 2.4. To be more specific, the stuck-open and stuck-on fault model is used and faults are considered one at a time. It was

shown in [11, 20, 21] that the MTS obtained from the stuck-at fault model does not detect all the faults that are at a lower level of abstraction.

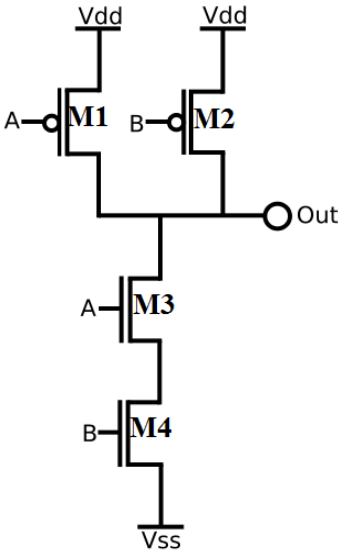

Figure 2.4: CMOS Two-input NAND Schematic

In [20], it was proven that SOP faults require a specific sequence of test vectors in order to be detected. Consider, for instance, the fault M1 SOP; this fault causes the output node to be floating and the output in this scenario can take the logic value of its previous output. Table 2.2 shows a test sequence that does not detect the fault M1 SOP. "HI" in the table explains that the output is floating and can take the value of its previous output.

Table 2.2: M1 SOP Undetected

A	B	Fault-Free output	Faulty Output
1	0	1	1
0	1	1	1 (HI pertains previous output)
1	1	0	0

However, the sequence of the input vectors shown in Table 2.3 detects the fault M1 SOP.

Table 2.3: M1 SOP Detected

A	B	NAND Fault-Free Output	NAND Faulty Output
1	0	1	1
1	1	0	0
0	1	1	**0 (HI pertains previous output)**

Table 2.4 states the appropriate input sequences that detect SOP faults in all transistors.

Table 2.4: Sequence Detecting SOP faults in all Transistors

SOP Fault	Test Sequence
M1	11,01
M2	11,10
M3 and M4	10,11 or 01,11

It can be clearly shown that a specific sequence of input vectors is required to detect stuck open faults. A possible test sequence is {11,01,11,10}. It is clear from the test sequence that only three test vectors are needed but one of them is repeated twice resulting in four ordered test vectors. This takes more time during the testing process when compared to the MTS obtained from the stuck-at fault model that does not include any test sequence. However, this is more accurate and has no test escapes.

Additionally, in [21] it was also shown that detecting resistive open faults usually modeled as R_{open} depends on the speed of test vector application. Consider the inverter chain shown in Fig. 2.5.

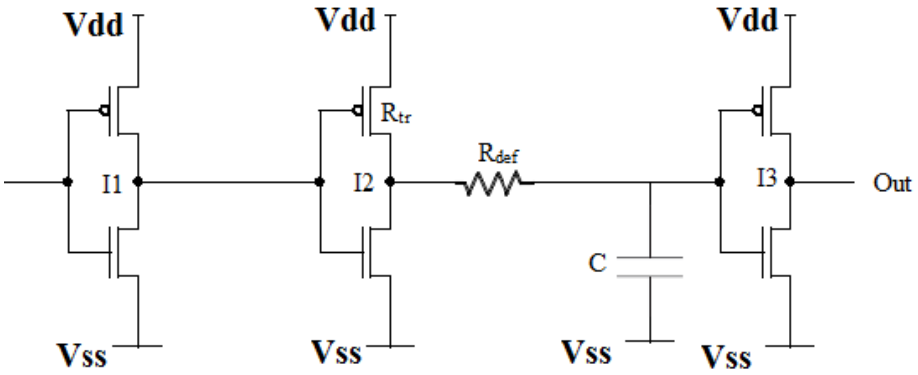

Figure 2.5: Inverter Chain

The delay of the inverter labeled I2 can be estimated by (2.1).

$$Delay \cong [R_{tr} + R_{def}].C \tag{2.1}$$

Another well-known family of designing digital logic gates is the Complementary Pass-Transistor Logic (CPL). In [22], testing of two-input AND/NAND, OR/NOR and XOR/XNOR designed using this family was tested for stuck-open and stuck-on faults. It was shown that test sequence should be considered to detect stuck open faults. The explanation of requiring test sequence is similar to that of testing CMOS circuits shown above.

This proves that using fault models at a low level of abstraction is more accurate but is more complicated and includes a higher number of faults considered in the fault list. As it was shown, the stuck-at fault model (gate level fault model) did not include information regarding test sequence or the test speed. These appeared when the transistor level fault model was used.

Chapter 3 next, focuses on testing an analog circuit, namely, CCII. CCII is a versatile analog building block used to implement various functionalities such as voltage follower, current follower and voltage-current converter. The CCII is tested using the DC Testing technique and the five-fault model is used. The fact that CCII could be used as a voltage-current converter is utilized to obtain the highest possible fault coverage.

Chapter 3

High Coverage Test for the Second Generation Current Conveyor

This chapter starts by giving an overview about current conveyors. This overview provides an explanation of what are current conveyors and it also includes several applications of current conveyors. Followed by that, a detailed description of a current conveyor circuit is provided. This is the circuit under test (CUT) where the test results of the second generation current conveyor (CCII) circuit are displayed. Furthermore, a detailed analysis of these results is provided. Conclusions are given at the end of this chapter.

3.1 Current Conveyors

Current Conveyors (CCs) were first introduced by Sedra and Smith in 1968 [1]. They were modified by the same authors two years later and named second generation current conveyors (CCIIs) [2]. As shown in the block diagram in Fig 3.1, CCII is a three terminal device defined by the matrix equation:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \tag{3.1}$$

where "±" indicates positive and negative current, respectively [2]. Positive current conveyors are known as CCII+ and vice versa.

From (3.1), the terminal impedance at ports Y and Z must be high. On the other hand, the terminal impedance of port X must be low. Moreover, port X can be used as an input current port or output voltage port [2, 23].

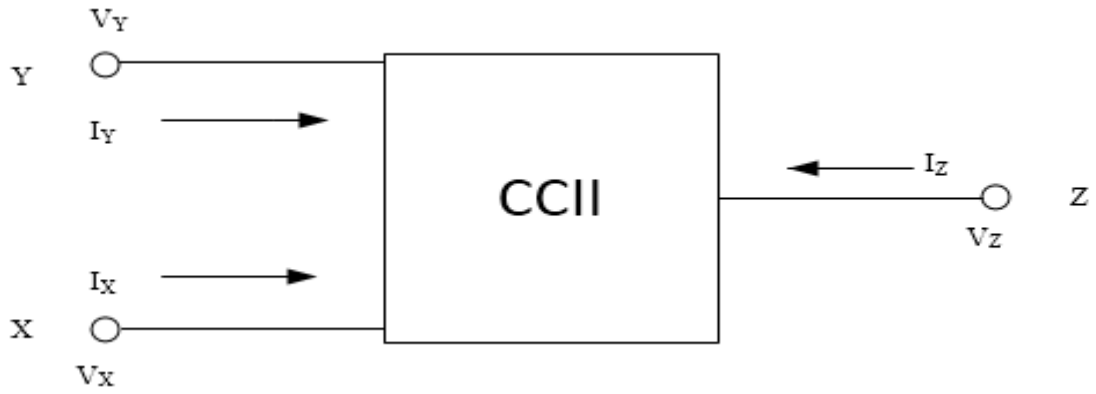

Figure 3.1: Second generation current conveyor

Since 1970, it has been proven that CCIIs are versatile building block in analog circuits [23]. CCIIs are used in current mode signal processing especially in low power and low voltage applications. It is a very useful block because it can perform analog applications by a suitable connection of one or more CCIIs with active and passive elements [1, 2]. CCIIs are used in digital to analog converters to provide output current source [23]. Moreover, it is used in applications such as oscillators, filters and amplifiers [24]. It is also used as an active building block in active capacitance multipliers, V-I scalar circuits and Biquadratic filters [25-27]. Many more applications of CCIIs are mentioned in [28].

To the best of our knowledge, the production testing of CCII+ has not been tackled in the literature. Consequently, a cost-effective technique for testing CCII+ is needed that produces high fault coverage.

3.2 Circuit Under Test Theory of Operation

CCII+ is implemented as shown in Fig 3.2, which was proposed in [23]. This circuit structure is the CMOS-based version of the bipolar based voltage to current converter proposed in [29]. Assuming transistors M1 and M2, M3 and M4 and M6 and M7 are well matched, current mirrors have a gain of 1 and all the transistors operate in the saturation region. The theory of operation is as follows. The current mirror M3-M4 forces an equal amount of current to flow into transistors M1 and M2, i.e., $I_{M1}=I_{M2}$. This forces gate-source voltages to be equal, i.e., $V_{gs1}=V_{gs2}$. As transistors M1 and M2 share the same source, the voltage at port X will follow the voltage at port Y, or $V_X=V_Y$. Transistors M5,

M6 and M7 are responsible for conveying current from port X to port Z. As the drain and source currents of M5 are equal and current mirror M6-M7 has a unity gain, i.e., $I_{M5}=I_C$, then $I_Z=I_X$. Transistors M8, M9 and M10 act as current sources [23].

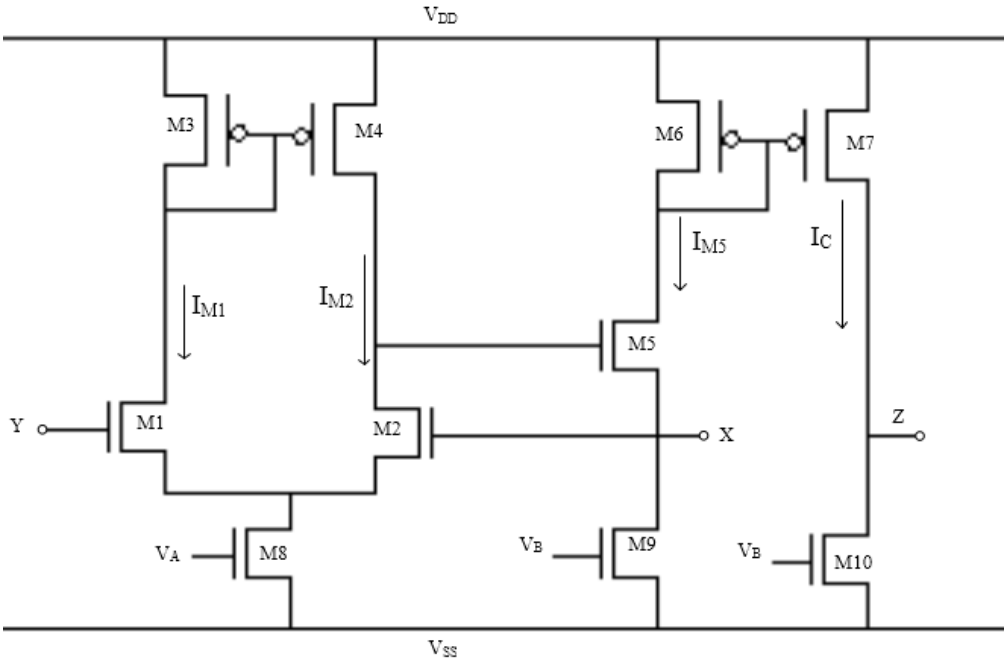

Figure 3.2: CCII+ CMOS Schematic

3.3 Production Testing of the CCII

Testing of the CCII+ circuit shown in Fig 3.2 is investigated. The ELDO simulator from Mentor Graphics is used in the study and the technology used is the 45nm CMOS technology. V_{DD} is 1V and V_{SS} is 0V. The biasing voltages V_A and V_B are 0.32V and 0.57V respectively. In this paper, the five-fault model proposed in [14, 15] is used, as it is one of the most commonly used fault models. The five-fault model consists of five faults per transistor which are: Drain-Source short circuit (DS), Gate-Drain short circuit (GD), Gate-Source short circuit (GS), Open Drain (OD) and Open Source (OS). It was shown in [30] that open circuit faults can be modeled by inserting a 250MΩ resistance or more, while short circuit faults are modeled by inserting a 10Ω resistance. The fault is detected if there is a deviation in the circuit response by more than ± 10% of the circuit response under fault free conditions as in [14]. This section investigates testing of the CCII under

three different testing setups: voltage follower, current follower and voltage to current converter.

3.3.1 Voltage Follower

To implement a voltage follower using CCII+, port Z must be grounded and port X is open circuited to observe the voltage transfer characteristics as in [31]. The five-fault model is applied to the circuit. The total number of transistors for the circuit under test is 10 transistors, which means that a total of 50 faults have to be considered. Faults are injected one at a time. DC testing is used to detect faults in the circuit. The input voltage V_Y is swept from 0V to 1V, i.e., from V_{SS} to V_{DD} and the output voltage V_X is observed.

Simulation results show that there are 13 undetected faults. 6 out of the 13 faults are dropped from the fault list, as they do not have a noticeable effect on circuit performance as in [32]. These faults are denoted by "X" in Table 3.1. For instance, the fault M8 GS is undetected because M8 will still act as the sink for the currents flowing in transistors M1 and M2. Despite the presence of this fault, Transistor M8 will function correctly, i.e., similar to the fault free scenario. The reason is that the applied gate bias voltage V_A is not merely shorted to the ground. However, it is connected to the ground through a 10Ω resistor representing the GS fault. V_A will be the drop across this resistor. By the same token, M9 GS and M10 GS are removed from the fault list. M8 DS is removed from the fault list because the circuit will be pulled down to ground at the source terminals of transistors M1 and M2. As a result, it is omitted from the fault list because the operation is not affected. The aforementioned faults are quite similar to the faults dropped from the fault list in [30]. Another two faults that are removed from the fault list are M3 GD and M6 GD. Under fault-free conditions, the gates of M3 and M6 are connected to their drains to implement current mirrors. So inserting M3 GD or M6 GD faults does not affect the circuit functionality. Therefore, they are dropped from the fault list. In total, 6 faults are removed from the 50 faults originally assumed.

For all the Tables following in this chapter, D indicates detected fault, U indicates undetected fault and X indicates a fault that is dropped from the fault list.

Table 3.1: Voltage Follower Test Results

Transistor	Faults				
	DS	**GD**	**GS**	**OD**	**OS**
M1, M2, M4 and M5	**D**	**D**	**D**	**D**	**D**
M3 and M6	**D**	X	**D**	**D**	**D**
M7	U	**D**	**D**	U	U
M8	X	**D**	X	**D**	**D**
M9	**D**	**D**	X	**D**	**D**
M10	U	U	X	U	U

All faults in transistor M10 are undetected. This is expected because the drain of M10, i.e., port Z is connected to ground as mentioned before. In addition, transistor M10 is not responsible for copying voltage from port Y to port X.

The fault M7 OS is undetected because transistor M7 is only responsible for conveying current from port X to port Z. M7 ensures that $I_{M5}=I_C$, which has nothing to do with copying voltage from port X to port Y. The same explanation can be given for M7 OD and M7 DS. Even though transistor M7 does not affect the voltage following functionality, M7 GS and M7 GD faults are detected. The explanation is as follows. As the drain of M7 is grounded and the fault M7 GD is injected, the voltage level at the gate of M6 is very low, i.e., close to V_{SS} value. Since the gate and drain of M6 are originally connected to implement a current mirror, the output voltage at port X will be low compared to that of the fault free conditions as shown in Fig 3.3.

For M2 GD fault, the current mirror M3-M4 will function normally. However, the current flowing into transistor M1 is not equal to that flowing into transistor M2 due to the presence of resistance between the gate and drain of transistor M2.

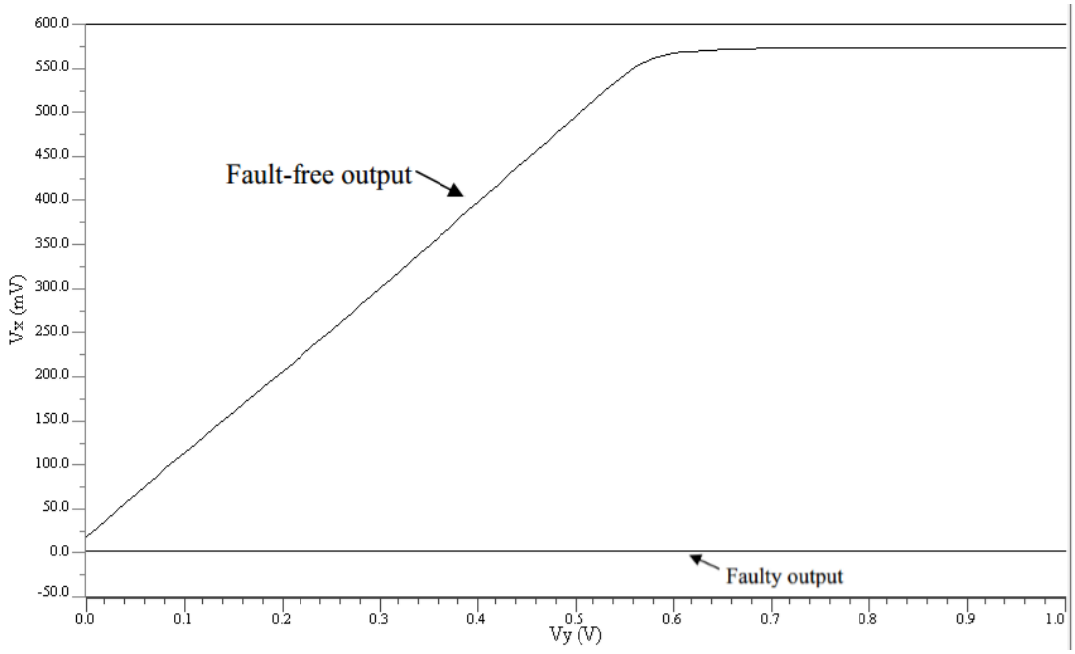

Figure 3.3: M7 GD Fault

In order to have voltage following from port Y to port X, currents flowing into transistors M1 and M2 must be equal and this is not the case when the fault is inserted. Hence the voltage following action will not occur and the fault is detected. The results of the aforementioned fault are shown in Fig. 3.4.

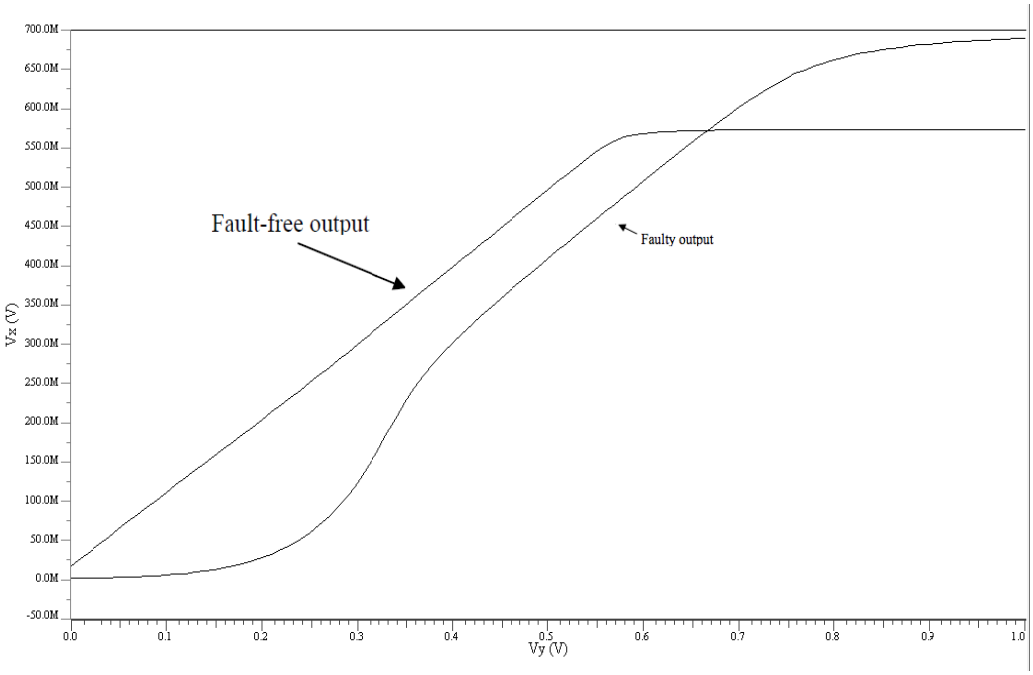

Figure 3.4: M2 GD Fault

In summary, it was shown that out of 50 faults, 6 are dropped from the fault list since they do not affect the operation of the circuit. So, the fault list has a total of 44 faults. Out of the 44 faults, 37 faults are detected by the test values 0V and 1V. This results in a total fault coverage of 84.1%.

3.3.2 Current Follower

To implement a current follower using CCII+, port Y is grounded to observe the current transfer characteristics as in [2]. The five-fault model is applied. Faults are injected one at a time. The input current I_X is swept from 0μA to 5μA and the output current I_Z is measured.

Simulation results show that there are 7 undetected faults. 6 faults of the 7 are dropped from the fault list as they do not have a noticeable effect on the circuit performance as explained before in section 3.3.1. These faults are denoted by "X" in Table 3.2.

Table 3.2: Current Follower Test Results

Transistor	**Faults**				
	DS	**GD**	**GS**	**OD**	**OS**
M1	**D**	**D**	U	**D**	**D**
M2, M4, M5 and M7	**D**	**D**	**D**	**D**	**D**
M3 and M6	**D**	X	**D**	**D**	**D**
M8	X	**D**	X	**D**	**D**
M9 and M10	**D**	**D**	X	**D**	**D**

M1 GS fault does not affect the current transfer characteristics as it is not responsible for conveying current from port X to port Z. Therefore, it cannot be detected by observing the output current I_Z. This fault causes transistor M1 to be in the cut-off region. So the current I_{M1} is too low. Hence, the input current I_Y will be negligible. I_Y

under fault free conditions is zero. Therefore, it cannot be detected by monitoring the input current I_Y.

The fault M7 OS corrupts the functionality of the current mirror M6-M7. As a result $I_C << I_{M5}$ due to the presence of a high resistance value between the source of transistor M7 and the supply. Hence, the output current I_Z will be much lower than it should be under fault free conditions. Therefore the fault is detected.

In summary, it is shown that 43 faults are detected out of the 44 faults yielding 97.7% fault coverage. This coverage is achieved by the test value 0μA.

3.3.3 Voltage-Current Converter

In order to implement a voltage to current converter, a converting resistor R_{XL} is placed between port X and the ground [22]. R_{XL} should be large enough to have a linear system. In this study, R_{XL} is set to be 200KΩ. The input voltage V_Y is swept from 0V to 1V, i.e., V_{SS} to V_{DD}, while observing the output current I_Z. Equation (3.2) shows how input voltage is converted to output current using CCII+ [23].

$$I_X = I_Z = \frac{V_Y}{R_{XL}} \tag{3.2}$$

The five-fault model is applied and faults are injected one at a time. In this mode of operation, the voltage and current transfer characteristics are examined. Simulation results show that there are 6 undetected faults. These faults are removed from the fault list for reasons explained in Section 3.3.1. They are denoted by "X" in Table 3.3.

The fault M9 DS causes port X to always have a fixed voltage of 0V irrespective of the input voltage V_Y. This corrupts the voltage following functionality, which in turn causes the whole process of converting input voltage to output current to malfunction. The results of the aforementioned fault are shown in Fig 3.5.

Table3.3: Voltage-Current Converter Test Results

Transistor	Faults				
	DS	**GD**	**GS**	**OD**	**OS**
M1, M2, M3, M4, M5 and M7	**D**	**D**	**D**	**D**	**D**
M3 and M6	**D**	X	**D**	X	D
M8	X	**D**	X	**D**	**D**
M9 and M10	**D**	**D**	X	**D**	**D**

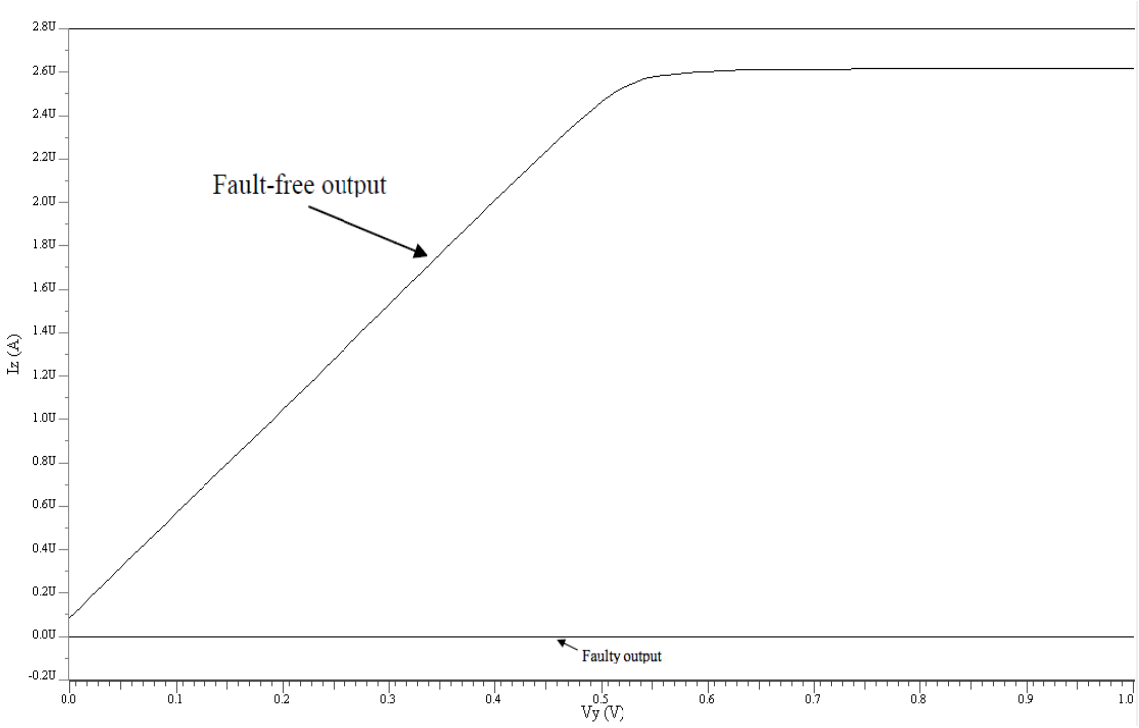

Figure 3.5: M9 DS Fault

In summary, it was shown in this subsection that 44 faults are detected by observing the output current I_Z using the test values 0V and 1V. Therefore, testing the circuit in the voltage to current converter mode yields a 100% fault coverage.

3.4 Summary

CCIIs are versatile building blocks in analog circuit design because analog applications can be implemented using suitable connections of one or more CCIIs with passive and active elements. Hence, it is essential to reduce the test cost/time of the CCII+ circuit, which is the goal of this study.

The technology used is the 45nm CMOS technology. The fault list consists of 50 faults as five faults are assumed for every transistor and faults are introduced one at a time. 6 faults are removed from the fault list as they do not have noticeable effect on the circuit functionality. The fault is considered detected if the deviation in the output response is more than $\pm$ 10% of the circuit response under fault free conditions.

Testing is investigated in three phases. The first phase is to test that $V_X=V_Y$, i.e., the voltage transfer characteristics. DC testing is applied. The input voltage is swept from 0V to 1V and the output voltage is observed. 37 faults are detected by the test values 0V and 1V. Hence, it is found that the fault coverage is 84.1%.

The current transfer characteristics are then studied. The input current I_X is swept from 0µA to 5µA and I_Z is monitored. It is found that the fault coverage increased to 97.7% and the test value is 0µA.

Finally, the third phase of testing the CCII+ is to investigate the voltage-current transfer characteristics. This is done by connecting a converting resistance R_{XL} between port X and ground. The output current at port Z is observed while the input voltage at port Y is swept from 0V to 1V. All the 44 faults are detected by monitoring the output current I_Z using the test values 0V and 1V. There fore, the fault coverage is 100%. Hence, it is recommended to test the CCII+ under voltage-current converter mode to obtain the highest coverage.

So far, testing of analog circuits has been addressed. The coming chapter investigates the testing of digital circuits that are implemented using memristors. Memristor is a new device used in many analog as well as digital applications. The chapter will be devoted to the study of memirstor-based circuits; more specifically MRL

will be studied and the focus will be on the production testing of two-input NAND and NOR logic gates.

Chapter 4

On the Production Testing of Memristor Ratioed Logic (MRL) Gates

This chapter starts by mentioning why memristors are needed. Then memristors are briefly introduced. Followed by that a description of how digital logic gates could be designed using memristive devices. Finally, the production testing of two-input NAND and NOR gates that are designed using the MRL family is presented.

4.1 Why Memristors are needed

Over the past decades, semiconductor technology has provided enormous enhancements in systems characteristics such as power consumption, speed, reliability and production cost. Such improvements came into practice mainly due to the continuous miniaturization of device dimensions in the fabrication process [33]. This incessant down scaling of devices leveraged the integration of more circuitry on a single chip producing complex hardware systems. However, this down scaling cannot take place forever. There are many factors that limit the down scaling of transistors such as the minimum dimensions that could be fabricated and increase in the off-state power consumption due to high leakage currents [33, 34]. Hence, innovations are required to allow for the continued growth in the complexity of hardware systems. One of these innovations is the memristors and memristive devices [33].

4.2 Memristors and MRL

Memristors existence were theoretically predicted in 1971 by Chua [3]. In 2008, Hewlett Packard (HP) physically realized the memristor [35]. The memristor uses thin film of Ti02 sandwiched between two Platinum contacts. The Ti02 film contains two regions. The first is a high conductance doped region while the second is a high resistance undoped region. When a positive voltage is applied across the device (current flowing into the device), the dopants drifts towards the undoped region, increasing the proportion of the

conductive region. Similarly, the application of negative voltage increases the resistance [35].

In other words a memristor is a resistive switch that produces, either a high resistance or a low resistance depending on the polarity of the applied voltage, i.e., the direction of current flow [33, 35]. Figure 4.1. shows the symbol and polarity of the memristor.

Memristors are mainly used in memories. In memories, memristors are used to represent logic states, i.e., the resistance of a memristor is used to represent logic 0 or logic 1. As of any other device, memristors are prone to defects. Numerous research efforts took place in testing memristor-based memory systems. In [36, 37], different fault models were proposed. [38], proposed two DfT schemes for testing memristors using these fault models and the conventional March test was used, in which a fixed pattern of reads and writes are applied to each memory cell to detect faults in that cell. This method (tests one cell at a time) is time consuming for large memories. Therefore, testing multiple transistors at the same time was needed. This was done by using divide-and-conquer testing technique proposed in [39, 40]. However, this technique does not consider sneak-paths (unwanted current flow) in crossbar memories. In [41], a sneak-path testing scheme was proposed to test multiple memristors simultaneously using sneak-path currents. In [42], a new design was proposed to overcome the issue of sneak path currents in memristor crossbar memories. The design is comprised of one access transistor and one memristor (1T1R). Fault models are proposed in [42], based on electrical defects. A March Test is proposed to cover all the defined faults.

Memristors are also used to design logic circuits where memristors are used as computational elements as in [33].

The coming paragraphs provide an explanation of the MRL logic family. In [33], MRL is used to design two-input NAND and NOR Boolean functions. The memristors are used to perform the AND and OR functionalities, while a standard CMOS inverter is used to obtain their complements. In [33], the TEAM (ThrEshold Adaptive Memristor) model was used.

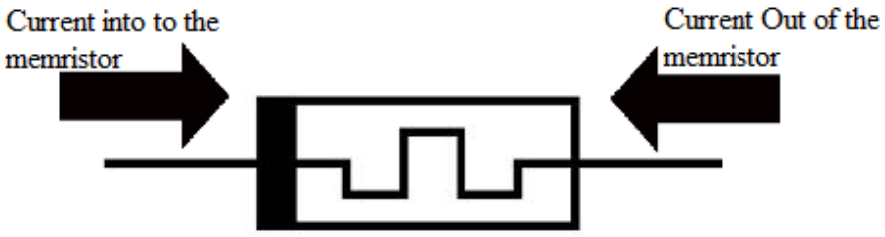

Figure 4.1: Memristor symbol. Thick black line on the left represents the polarity of the device. If current flows into the device, resistance of the memristor decreases and vice versa.

Two-input AND and OR logic gates consists of two memristors connected in series at opposite polarities as shown in Figs. 4.2a and 4.2b, respectively. The memristors are used as computational elements to evaluate logic. On one end of the memristors terminals the inputs A and B are applied, while the common node of the memristors is the output node labeled $V_{out,AND}$ and $V_{out,OR}$. The CMOS inverter is added then for reasons mentioned later.

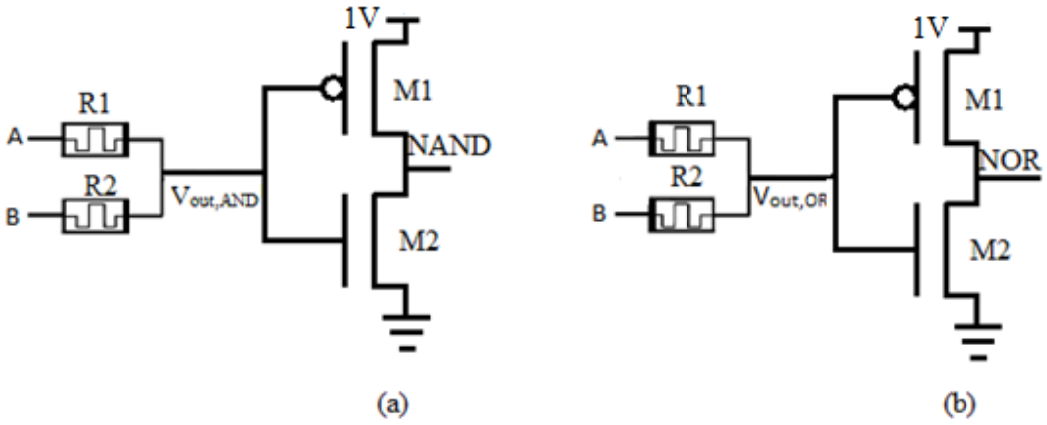

Figure 4.2: Schematic of (a) two-input MRL NAND (b) two-input MRL NOR

In the AND logic gate, when the current flows out of the memristors, the resistance of the memristors increases and reaches R_{off} eventually. On the other hand, if the current flows into the memristors, the resistance of the memristors decreases and reaches R_{on} eventually. The OR logic gate has the exact opposite behavior of the AND gate as opposite polarity is used.

In the following explanation, 0V is used to represent logic '0' and 1V is used to represent logic '1'. AND and OR logic gates behave similarly when identical inputs are applied, i.e., AB=00 or AB=11. When these inputs are applied, there is no current flow through the memristors. Hence, there is no voltage drop between the inputs. Therefore, the output voltage $V_{out,AND}$ and $V_{out,OR}$ are similar to the input voltage. In the case where the inputs are different, i.e., AB=01 or 10, current flows from the higher input voltage terminal to the lower. This changes the resistance of the two memristive devices.

In the AND logic gate, consider the input vector AB=10. For this case, the current flows out of memristor labeled R1 in Fig. 4.3a. R1 reaches R_{off} by the end of the computational process. Simultaneously, the current flows into memristor labeled R2 in Fig. 4.2a and R2 reaches R_{on} towards the end of the logic evaluation. The output voltage $V_{out,AND}$ is a voltage divider between the two memristors, and is therefore

$$V_{out.AND} = \frac{R_{on}}{R_{off} + R_{on}} \times 1V \approx 0V \tag{4.1}$$

Consider the same scenario AB=10 for the OR logic gate, where opposite polarity is used. Therefore, the resistance of the memristors behave in the exact opposite way of the AND logic gate and the output voltage $V_{out,OR}$ is therefore

$$V_{out,OR} = \frac{R_{off}}{R_{off} + R_{on}} \times 1V \approx 1V \tag{4.2}$$

It should be noted that the initial resistance of both memristors does not affect the functionality. However, it affects the delay of computation when both inputs are different [32]. A standard CMOS inverter is added for two main reasons. First, since the AND and OR functions are non-inverting, a complete logic structure is achieved by connecting the output node to a CMOS inverter. In addition, memristive devices lack signal restoration, i.e., the output voltage levels will degrade if these logic gates are cascaded for several levels [32].

4.3 Production Testing of two-input NAND and NOR MRL Gates

This section investigates production testing for catastrophic faults in the MRL NAND and NOR logic gates shown in Figs. 4.2a and 4.2b, respectively. MRL uses

memristors and transistors to build logic gates. Therefore, faults that occur in both memristors and transistors are considered.

In this research, the TEAM model is used as this model was used by [33] in the proposed designs. The ELDO simulator from Mentor Graphics is used in this study and the technology is the 45nm CMOS technology.

The memristor stuck-at fault model proposed in [36] is used. As memristors depends on doping, the following defects could occur:

(l) Stuck at 1 defect (SAl):

If Ti02 is doped excessively with positively charged oxygen vacancies, the memristor remains stuck in the ON state, even when a negative voltage is applied across the memristor. Hence the memristor obtains a low resistive state of R_{on}.

(2) Stuck at 0 defect (SA0):

If Ti02 is deficient of positively charged oxygen vacancies, the memristor remains stuck in the OFF state, even when a positive voltage is applied across the memristor. Hence the memristor obtains a high resistive state of R_{off}.

This fault model assumes that the resistance of the memristor will remain stuck at either R_{on} or R_{off} irrespective of the applied voltage across its terminals. (put more about memristor fault models) According to the TEAM model parameters, R_{on} is 100Ω and R_{off} is 200KΩ. In addition, the transistor five-fault model proposed in [14, 15] is used, as it is one of the most commonly used transistor level fault models. The five-fault model consists of five faults per transistor which are: Drain-Source short circuit (DS), Gate-Drain short circuit (GD), Gate-Source short circuit (GS), Open Drain (OD) and Open Source (OS). It was shown in [30] that open circuit faults can be modeled by inserting a 250MΩ (or more) resistance in the 45nm technology, while short circuit faults are modeled by inserting a 10Ω resistance. Faults are injected one at a time as in [43]. For every fault, the circuit output is compared to the fault-free output. A fault is considered detected if the output is different from the fault-free case. Faults in the memristors are first studied followed by that resistive open and resistive short faults in the transistors.

4.4 Memristor Faults

In this section, memristor faults are considered for both the NAND and NOR logic gates.

The standard CMOS inverter used in Figs. 4.3a and 4.3b has a switching threshold voltage (V_M) of 0.5V. $V_{out,AND}$ and $V_{out,OR}$ (input nodes of the inverter) may be affected by noise that is taken as 5% of the supply voltage (1V), i.e., 0.05V as in [44]. Hence any input voltage to the inverter that falls between 0.45V and 0.55V is considered to be undefined. For the NAND and NOR logic gates, it is observed that, due to faults in the memristors, the output voltage $V_{out,AND}$ and $V_{out,OR}$ falls in the undefined region for some input vectors. Therefore, it is considered here that these input vectors that produce an output in the undefined region, cannot be used as test vectors.

For the NAND logic gate, consider for example, the fault R1 stuck-at R_{off}; it is clear from Fig. 4.3 that all test vectors produce the correct output except the test vector AB=01. This input vector produces an output of 0.5V that falls in the undefined region.

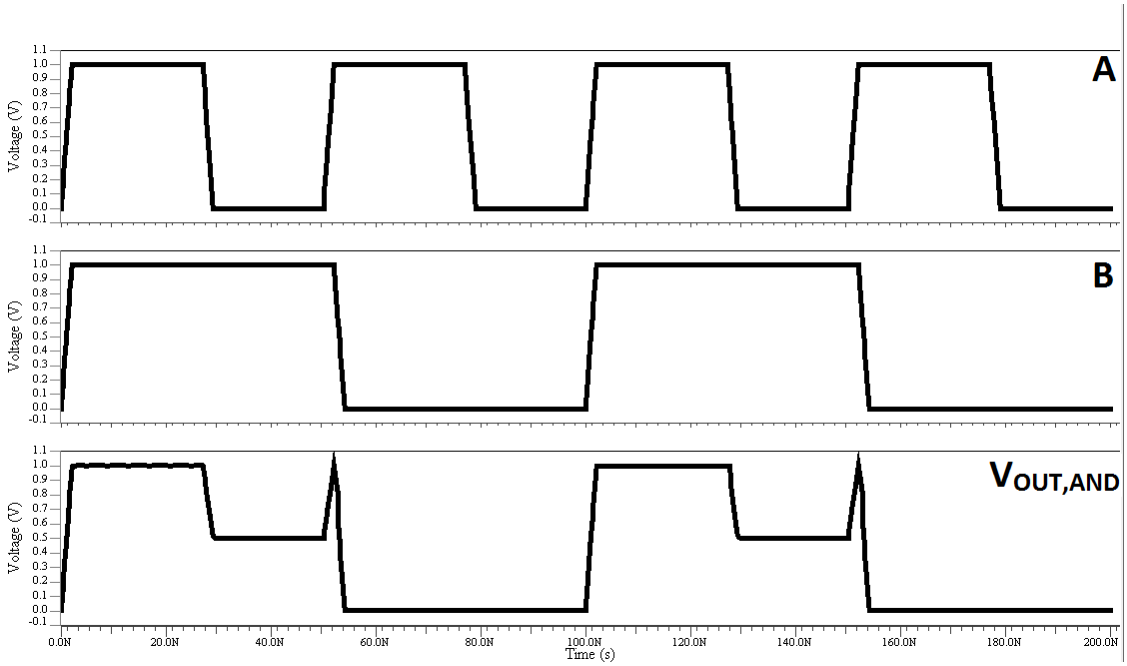

Figure 4.3. Test Results for R1 stuck-at R_{off} for the NAND Gate

The explanation of this result is as follows. Applying the test vector '01' forces R1

to switch to R_{on} and R2 should switch to R_{off} by the end of the computation process. However, due to the fault, R1 does not switch to R_{on} and is stuck at R_{off}. Hence the output voltage $V_{out,AND}$ is therefore 0.5V from (4.3).

$$V_{out,AND} = \frac{R_{off}}{R_{off} + R_{off}} \times 1V = 0.5V \tag{4.3}$$

Likewise, the same issue of output voltages falling in the undefined region occurs in the NOR logic gate. Consider, For example, the fault R2 stuck-at R_{on}, it is clear from Fig. 4.4 that all test vectors produce the correct output except the test vector AB=10. This input vector produces an output of 0.5V that falls in the undefined region as shown.

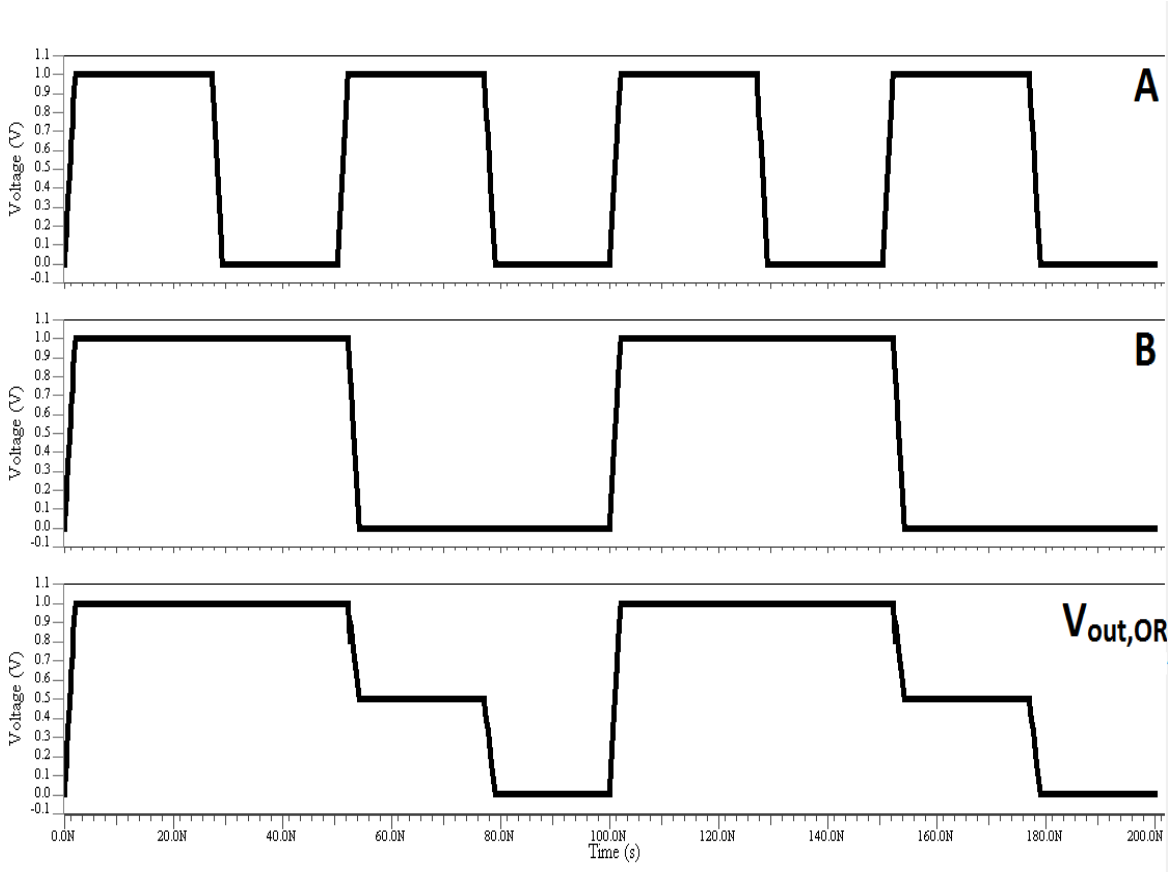

Figure 4.4: Test Results for R2 stuck-at R_{on} for the NOR Gate

Therefore, there are two different proposed solutions to the aforementioned issue as shown in the coming subsections.

4.4.1 Scaled Input Voltages

The first proposed solution is applying scaled input voltages to the inputs of the logic gates to detect all memristor faults. For the NAND logic gate, 0.33V is used to represent logic low '0' while keeping logic high '1' represented by 1V. This forces the output voltage $V_{out,AND}$ to be 0.67V (midpoint between 0.33V and 1V) for the same fault ($R1 \rightarrow R_{off}$), which is interpreted by the CMOS inverter as logic high '1' (0.67V is not in the undefined region); so the NAND output is logic low '0' and the fault is detected. Table 4.1 shows the test results for the NAND gate where logic low '0' is 0.33V and logic high '1' is 1V. Note that in Table 4.1, 'D' indicates a detected fault while 'U' indicates undetected fault. Also $R \rightarrow R_{on}$ indicates that the resistance of the memristor is stuck at R_{on} and $R \rightarrow R_{off}$ indicates that the resistance of the memristor is stuck at R_{off}.

Table 4.1: MRL NAND Test Results

Input Vector <AB>	**Faults**			
	$R1 \rightarrow R_{on}$	**$R1 \rightarrow R_{off}$**	**$R2 \rightarrow R_{on}$**	**$R2 \rightarrow R_{off}$**
00	U	U	U	U
01	U	**D**	**D**	U
10	**D**	U	U	**D**
11	U	U	U	U

In the NOR gate, the solution is keeping 0V to represent the logic low '0' while logic high '1' should be represented by 0.67V. Table 4.2 shows the test results for the MRL NOR gate. Note that in Table 4.2, 'D' indicates a detected fault while 'U' indicates undetected fault. Also $R \rightarrow R_{on}$ indicates that the resistance of the memristor is stuck at R_{on} and $R \rightarrow R_{off}$ indicates that the resistance of the memristor is stuck at R_{off}.

Table 4.2: MRL NOR Test Results

Input Vector <AB>	**Faults**			
	$R1 \rightarrow R_{on}$	**$R1 \rightarrow R_{off}$**	**$R2 \rightarrow R_{on}$**	**$R2 \rightarrow R_{off}$**
00	U	U	U	U
01	**D**	U	U	**D**
10	U	**D**	**D**	U
11	U	U	U	U

It is clearly observed from Tables 4.1 and 4.2 that only two test vectors 01 and 10 are needed to detect the memristor faults. It is expected that the test vectors 00 and 11 do not detect faults because there is no current flow in or out of the memristors when these vectors are applied; there is no voltage drop between the inputs, and $V_{out,AND}$ and $V_{out,OR}$ will be similar to the input voltage irrespective of the memristors state.

4.4.2 Changing the Switching Threshold of the Inverter

The second proposed solution is changing V_M of the inverters, by carefully sizing the PMOS and NMOS transistors. For the NAND logic gate, the inverter is designed to have V_M of 0.35V. Consider the same fault R1→R_{off} for the same input vector AB=01; this fault causes the input of the inverter $V_{out,AND}$ to be 0.5V which is interpreted by the inverter as logic high '1' so the NAND output is logic low '0' and the fault is detected. The test results are identical to those shown in Table 4.1. For the NOR logic gate, the inverter is designed to have V_M of 0.65V. The test results are identical to those shown in Table 4.2. Table 4.3 shows a summary of the V_M and the undefined region of the three different CMOS inverters.

Table 4.3: Summary of V_M and the undefined region of three different inverters

	Standard Inverter	**Low V_M Inverter (NAND)**	**High V_M Inverter (NOR)**
V_M	0.5V	0.35V	0.65V
Undefined Region	0.45V-0.55V	0.3V-0.4V	0.6V-0.7V

4.5: Resistive Open Faults in NAND and NOR

In this subsection, detection of resistive open faults is shown. It is observed that detecting resistive open faults depend on the speed of test vector application and the order of application of the test vectors. It was shown in [21] that detecting resistive open faults depends on the speed of test vector application. For the NAND logic gate in Fig 4.3a, consider, for example, the fault M1 OD, i.e., resistive open in transistor M1. For the input

vectors 01 or 10, an RC circuit is established between the supply voltage V_{dd} and the NAND output node. R is R_{M1}, which is the equivalent ON resistance of the PMOS transistor M1 in series with R_{op}, which is the injected fault. C represents the overhead capacitance. In this case the delay of the inverter can be estimated by (4.4) as in [21]:

$$Delay \cong [R_{M1} + R_{op}].C \tag{4.4}$$

Therefore, if the test speed is very slow, i.e., enough time is given for logic evaluation and the fault will not be detected. This applies for both NAND and NOR gates.

Additionally, it was shown in [20], that testing resistive open faults in the CMOS NAND logic gate depends on the order of test vector application. It is concluded from [20], that although the minimum test set includes only three test vectors, namely 01,10 and 11, four input vectors have to be applied. For example, a possible test sequence might be 11, 01, 11, 10.

Likewise, detecting resistive open faults in NAND and NOR MRL family depends on the order of test vectors application. The coming two subsections discuss the test sequence needed for full fault coverage in NAND and NOR MRL family.

4.5.1 Detection of Resistive Open Faults for the Scaled Input Voltages Proposal

It is mentioned earlier in this chapter that input voltages are scaled to detect all memristor faults. It is found that detecting open faults depends on the order of test vector application. For instance, consider the fault M2 OD/OS for the NAND logic gate, i.e., resistive open in transistor M2 in Fig 4.3a. This fault isolates the NAND output from the ground voltage. So if the input vector applied is 11 the output node will also not be connected to the supply because this turns transistor M1 off. The output then is floating and retains its previous logic state as in [21]. In order to detect this fault, an initializing vector activating the pull up PMOS transistor M1 must be applied which is 01 or 10 in this case. Applying these test vectors 11 pulls up the output of the NAND gate to '1'. After applying the initializing vector, the test vector 11 is applied. This keeps the output

of the NAND gate in the floating state and will retain its previous logic state, which is '1' and hence the fault is detected. Table 4.4 shows test results of detecting open faults in transistors M1 and M2 for the MRL NAND gate. Unlike the previous fault, open faults in M1 do not require a specific sequence to be detected and can be detected by either 01 or 10. M1 OD/OS merely cuts the path for the supply voltage and, accordingly, M1 is unable to pull up the output node to '1'. When 01 or 10 is applied, bearing in mind that '0' is 0.33V, 0.33V (higher than the threshold of the transistor) is transmitted to the input of the inverter, switches M2 ON and the output node is pulled to ground. Hence, the fault is detected.

Table 4.4: Test Sequence/Vectors to Detect Open Faults in MRL NAND using Scaled Input Voltages

	M1 OD/OS	M2 OD/OS
Initializing Vector <AB>	Not Needed	01/10
Detecting Test Vector <AB>	01/10	11

The same explanation could be given for resistive opens in the NOR MRL logic gates. However, different test vectors are used with specific sequence as shown in Table 4.5.

Table 4.5: Test Sequence/Vectors to Detect Open Faults in MRL NOR using Scaled Input Voltages

	M1 OD/OS	**M2 OD/OS**
Initializing Vector <AB>	01/10	Not Needed
Detecting Test Vector <AB>	00	01/10

4.5.2 Detection of Resistive Open Faults for the Different Switching Thresholds of the Inverter Proposal

It is mentioned earlier in this chapter that changing V_M of the inverter is needed to detect all memristor faults. Order of test vector application is required for full fault coverage in this proposed solution. For instance, consider the fault M1 OD/OS for the NAND logic gate, i.e., resistive open in transistor M1 in Fig. 4.3a. This fault isolates the NAND output from the supply voltage. So if the input vector applied is 01 or 10 the

output node will also not be connected to ground because this turns transistor M2 off. The output then is floating and retains its previous logic state as in [21]. In order to detect this fault, an initializing vector activating the pull down NMOS transistor M1 must be applied which is 11 in this case. Applying the test vector 11 pulls down the output of the NAND gate to '0'. After applying the initializing vector, any of the other two test vectors 01 or 10 could be applied. This keeps the output of the NAND gate in the floating state and will retain its previous logic state, which is '0' and hence the fault is detected. The same explanation could be given for other resistive opens in the NAND and NOR MRL logic gates. Table 4.6 shows the test sequence required to detect open faults in transistors M1 and M2 for the MRL NAND gate.

Table 4.6: Test Sequence to Detect Open Faults in MRL NAND using Low V_M inverter

	M1 0D/OS	**M2 OD/OS**
Initializing Vector <AB>	11	01/10
Detecting Test Vector <AB>	01/10	11

The same explanation could be given for resistive opens in the NOR MRL logic gates. However, different test vectors are used with specific sequence as shown in Table 4.7.

Table 4.7: Test Sequence to Detect Open Faults in MRL NOR using High V_M inverter

	M1 0D/OS	**M2 OD/OS**
Initializing Vevtor <AB>	01/10	00
Detecting Test Vector <AB>	00	01/10

4.6 Resistive Short Faults in NAND and NOR

Resistive short faults test results for both the two-input NAND and NOR gates are presented in Tables 4.8 and 4.9, respectively. The results are identical for the two proposed solutions.

Table 4.8: Resistive Short Faults Test Results in MRL NAND

Transistor	Faults		
	DS	GD	GS
M1	11	00/01/10	00/01/10
M2	00/01/10	00/01/10	11

For the NAND MRL, consider, for instance, the Fault M1 DS, this forces the output node to always be logic high '1' as the node is shorted to the supply. Therefore, this fault is only detected by the test vector AB=11, where the output in the fault free scenario should have been logic low '0'. Figure 4.5 shows the test result of this fault.

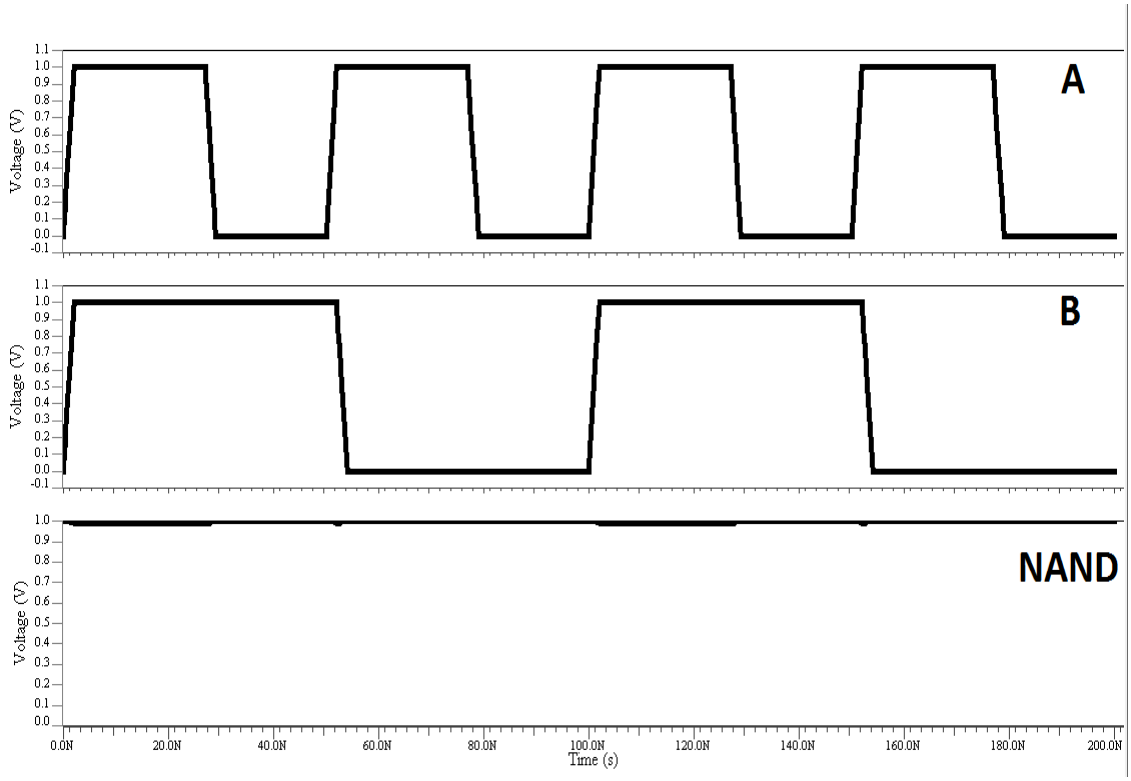

Figure 4.5: NAND M1 DS Fault

Table 4.9: Resistive Short Faults Test Results in MRL NOR

Transistor	Faults		
	DS	GD	GS
M1	01/10/11	01/10/11	00
M2	00	01/10/11	01/10/11

For the NOR MRL, consider, for instance, the Fault M2 GS, this forces the input node of the inverter to always be a logic low ‘0’. This causes the output to be stuck-at logic high ‘1’. Therefore, this fault is detected by the test vectors that produce logic high ‘1’ at the input of the inverter (01/10/11), where the output in the fault free scenario should have been logic low ‘0’. Figure 4.6 shows the test result of the fault M2 GS.

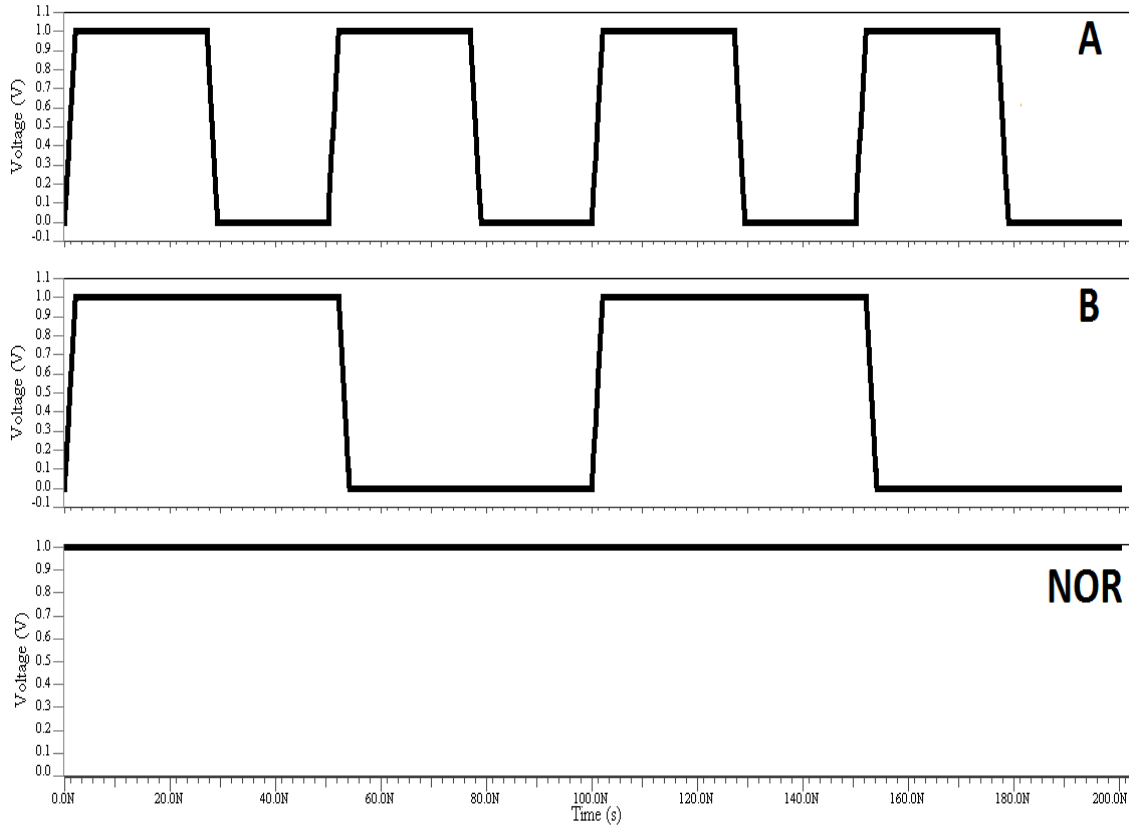

Figure 4.6: NOR M2 GS Fault

It is concluded from the test results shown in the tables above that, for the two proposals, the minimum test set required is identical to that obtained from the conventional single stuck-at fault model. However, it was shown that the order of applying the test vectors is important. A possible test pattern that obtains 100% fault coverage in NAND MRL gate is (10,11,01). This is a major difference between MRL NAND and CMOS NAND in that, despite both gates requiring the same three test vectors for full

coverage, MRL requires a sequence of three vectors while CMOS requires a sequence of four vectors. It is also concluded that detecting resistive open faults in MRL NAND/NOR gate depends on the test speed.

4.7 Summary

Memristors have been physically characterized in 2008 by HP. One of the main advantages of using memristors in memories, analog circuits, neuromorphic systems and digital circuits, is its area occupancy.

Memristors and CMOS inverters are integrated with each other to realize logic gates such as NAND, NOR and XOR. This design logic family is called MRL. The main advantage of this logic family is that it saves physical area and therefore increases logic density, which allows the increase of system complexity. Hence, it is important to test these gates efficiently.

In this study, the TEAM model and the 45nm CMOS technology were used. The memristor stuck-at fault model and the five-fault model are considered. Faults are injected one at a time. A fault is considered detected if the output is different than the fault-free output scenario.

During the testing of memristor faults, the input of the inverter falls in the undefined region and this might lead to test escapes. Therefore, two solutions were proposed to face this challenge. The first is to apply scaled input voltages and the second was to change the V_M of the inverter. It is shown that the minimum test set obtained in order to obtain full coverage for MRL NAND/NOR gates is identical to that obtained from the conventional single stuck-at fault model. However, the speed of applying the test vectors and the test order should be taken into account. Unlike CMOS NAND/NOR that require a sequence of four vectors for 100% fault coverage, MRL NAND/NOR require a sequence of only three test vectors.

Chapter 5

Conclusions and Future Work

We have tested a versatile analog building block, namely, CCII+. The CUT was tested for catastrophic faults using DC Testing technique. The five-fault model was used and faults were injected on at a time. Six faults were removed from the fault list as they did not have an effect on the circuit functionality. The fault was considered detected if the output due to the fault varies by $\pm$ 10% of the circuit response under fault free conditions. Testing was done on three different stages. First, the Voltage following functionality was tested and obtained a coverage of 84.1%. Followed by that, the current following functionality was observed and 97.7% fault coverage was achieved. The final stage was to test the ability of the CCII+ to convert input voltage into output current. This ensured that we are testing both voltage and current following functionalities simultaneously and full coverage was obtained using two test values. Hence, it was recommended to test the CCII+ under voltage-current converter mode to obtain the highest coverage.

Work in this area could be extended to test other realizations that were originally designed to achieve higher bandwidth using the same methodology followed in this dissertation.

Furthermore, testing digital logic gates that are implemented using memristors was investigated. The testing of two-input NAND and NOR gates were studied. The TEAM model and the 45nm CMOS technology were used. The memristor stuck at fault model and the five-fault model were considered and they were introduced one at a time.

One of the challenges faced when testing MRL gates is the appearance of voltage levels at the input of the inverter that fall in the undefined region. This might lead to some test escapes. Therefore, two solutions were proposed. One of the solutions is to apply scaled input voltages at the input terminals. The other solution was to change the V_M of the CMOS inverter to ensure 100% fault coverage.

It was concluded that the MTS required to test the two-input NAND and NOR MRL gates was identical to the MTS obtained from the stuck-at fault model. However, the speed of applying the test vectors and the test order should be taken into account. It was concluded that testing MRL gates require 3 ordered test vectors while testing CMOS gates require 4 ordered test vectors to detect all faults.

Work in this area could be extended to test multi-level gates or cascaded gates could be investigated as a line of research. Parametric faults could be studied as further research.

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