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Evaluation and implementation of a 5-level hybrid DC-DC converter

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THE AMERICAN UNIVERSITY IN CAIRO

SCHOOL OF SCEINCE AND ENGINEERING

EVALUATION AND IMPELEMENTATION OF A 5-LEVEL HYBRID DC-DC CONVERTER

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Abstract

School of Sciences and Engineering

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In this work, a hybrid voltage regulator topology is analyzed, implemented, and evaluated. The common topologies of DC-DC converters have proven to be lacking in some aspects, such as integrability for buck converters, or maximum efficiency for switched-capacitor regulators. The hybrid topology tackles these shortcomings by combining the advantages of switched-capacitor and inductor-based voltage regulators.

A 5-level buck converter is evaluated, implemented, and compared to other converter implementations using the same components. The 5-Level Buck converter can achieve 5 different levels, allowing it to cover 4 operation regions, each between 2 levels. Accordingly, it covers a wide range of output voltages. By reducing the voltage difference at the inductor input, the 5-level buck converter can use smaller inductor compared to both 3-level and conventional buck converters which makes it cheaper, smaller in size, and much more efficient. Simulations show proper functionality of the 5-Level topology, while putting restrictions on the inductor size, efficiency, and component footprint (or total converter area).

A test PCB is implemented for verification of the functionality and experimental measurements show that for the same switching frequency and inductor size, the 5-level buck converter achieves up to 15% efficiency improvement over a conventional buck converter and a 3-level buck converter at certain output voltage ranges. Peak efficiency of 94% has been

achieved by the 5-Level hybrid converter, which includes all external switching and conduction losses. The proposed hybrid topology proved to yield high conversion efficiency even in the face of component size limitations, which indicates potential benefit in using multilevel converters for several off-chip as well as on-chip applications.

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LIST OF ABBREVIATIONS

DC	Direct Current
PCB	Printed Circuit Board
POL	Point-of-Load
MEP	Minimum Energy Point
RF	Radio Frequency
VR	Voltage Regulator
UDVS	Ultra Dynamic Voltage Scaling
SCVR	Switched Capacitor Voltage Regulator
LDR	Low Dropout Regulator
PFM	Pulse Frequency Modulation
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
MOSFET	Metal-Oxide Silicon Field-Effect Transistor
ESR	Equivalent Series Resistance
FSL	Fast Switching Limit
SSL	Slow Switching Limit
FPGA	Field-Programmable-Gate-Array

Chapter 1

INTRODUCTION

1.1 Motivation

With the increasing advances in technology, several trends have dominated the electronics industry. One such trend is the reduction of size, and the increase in performance of consumer electronic devices. These advancements in size, performance, and power efficiency are the pillars of the move towards mobile devices, driving them to become more powerful, smaller, and lighter.

Accordingly, portable devices have become the new norm in modern day consumer electronics. Devices such as mobiles, tablets, and laptops are continuously being improved in order to compete in what has grown into a billion dollar industry. The market for these devices has even expanded to be the dominant type of consumer electronics. This driving force has molded the scientific community's incentives towards rapidly advancing modern technology to keep up with the increasing demand and growing market size. The main limitation to the continuing advancement in mobile devices is power management.

Mobile devices, tablets, and laptops are generally battery powered, and their processing modules are power sensitive. This creates a difficulty since the battery output voltage decreases as it is discharged over time. Accordingly, a voltage regulation mechanism is essential, which is satisfied by the use of bulky DC-DC converters. These converters also have high requirements on efficiency and power rating in order to obtain high power conversion while maintaining long battery lifetime.

The DC-DC converter is then one of the main components in a power management module, and the bulkiest, due to the use of large inductors, and the need for several converters within the device. For instance, Figure 1.1 shows a laptop's motherboard, which is dominated by power management modules, including the eight different DC-DC converters in the voltage supplies and the battery charger [1].

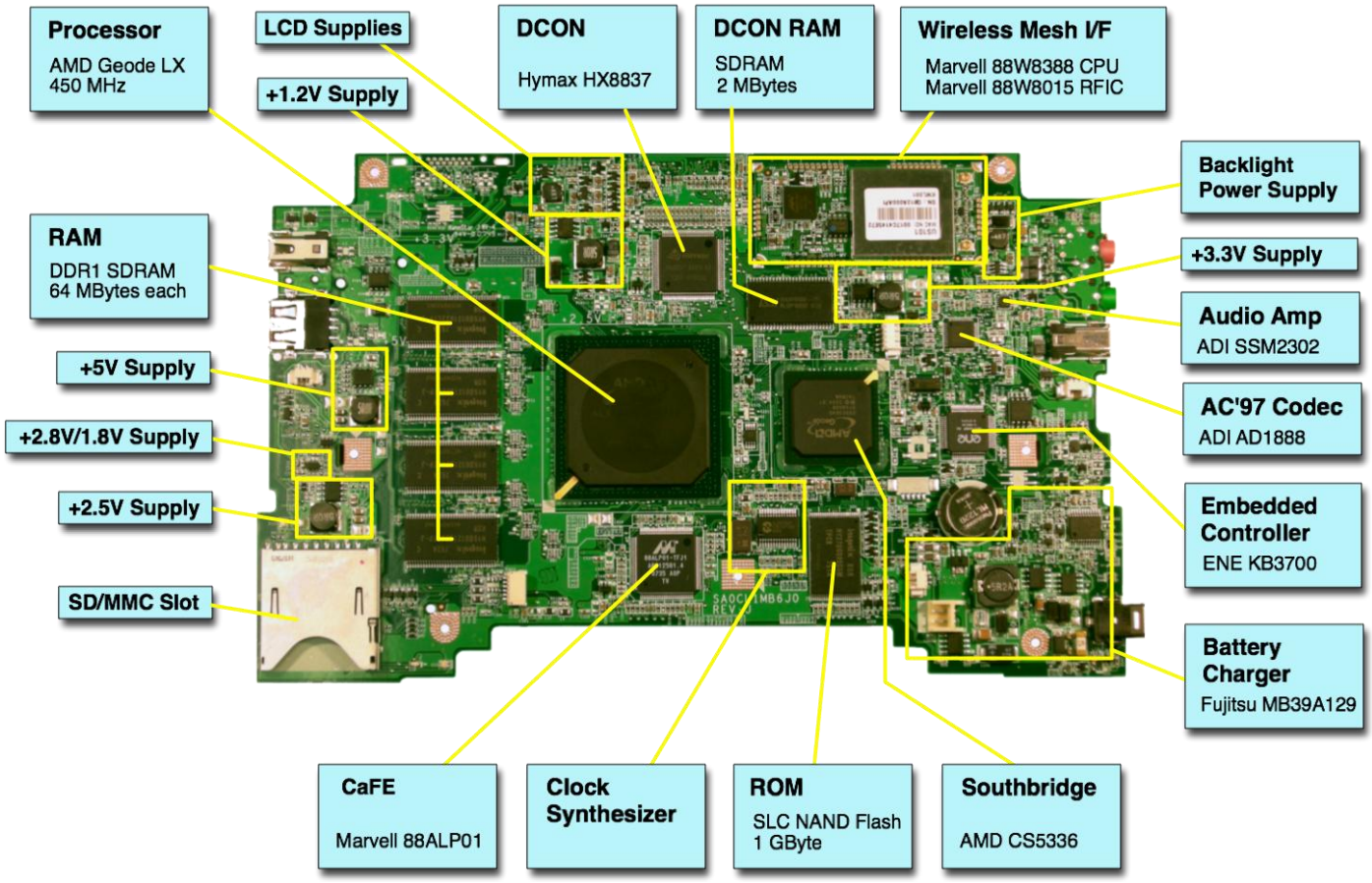

Figure 1.1: OLPC XO Laptop Motherboard [1].

The multitude of DC-DC converters in one motherboard is caused by the trend of placing the converter at the point of load (POL), which enables the transfer of the intermediate bus voltage into the voltage required by the particular load [2]. POL converters allow a significant reduction in voltage drops across power distribution networks, and in turn, increased efficiency. However, using multiple POL converters also leads to increased area. One method of overcoming this challenge is the use of compact DC-DC converters with minimally-sized components. It is shown in Figure 1.1 that the component dominating the area of each converter is the inductor, as it occupies about 25% of the total area of the 2.5V supply, 50% of the total area of the 5V supply, and 30% of the total area of the 3.3V supply. It is predicted that the number of supply voltages within the motherboard, and even the integrated circuit (IC), is increasing since different modules utilize different voltages to reach their maximum performance with highest efficiency [3]. Since the largest component in the DC-DC converters is the inductor, reducing its size needs to be prioritized in order to effectively minimize the total converter size.

Another demand for DC-DC converters, aside than compact size, is programmability, which allows varying the output voltage of the converter. This was implemented a number of times in the literature, due to its usefulness [4]. Programmable DC-DC converters have been implemented in small areas, in order to remain relevant for use in portable and handheld applications [5] [6]. Several regulation control methods have been implemented where the target has been dynamic performance through the optimization of the supply voltage [7]. It has also been used to obtain a lower voltage for standby mode in some applications, in order to minimize static power consumption, and to increase the supply voltage when the application is active and requires higher performance.

The need for an ultradynamic, fast response regulator is one of the main forces pushing for more research into DC-DC converters with increased performance. Ultradynamic, fast regulators are useful when considering low-power applications with minimum energy requirements. These applications contain logic elements that calculate the optimum supply voltage required for the application to function with the least power consumption.

One main method of optimizing the voltage supply to satisfy the performance and power consumption needs is to change it according to a weighted algorithm, where higher performance would require a higher supply voltage, at the expense of power consumption. On the other hand, a reduction in power consumption would require a lower supply voltage, at the expense of performance. There exists an operating voltage at which the total energy consumed by a digital circuit is minimized. This operating point, often referred to as the Minimum Energy Point (MEP), is only achievable with an ultradynamic regulator that can reach many supply voltages with minimal error, and with very small delay between two levels [8]. Tracking the MEP is currently a trend in modern circuits to optimize power consumption by dynamically changing the operating voltage to desired performance, which requires versatile DC-DC converters with large range of conversion ratios and with high performance throughout the range [7]. Changes in the MEP are based on factors such as load requirements and environmental conditions such as temperature. Energy savings due to MEP tracking have been reported to reach 50-100%, especially with circuits whose power losses are dominated by leakage.

Another application for ultradynamic DC-DC converters is envelope tracking for radio frequency (RF) applications [9]. These applications are very sensitive to voltage variations, and therefore require output voltage accuracy for envelope tracking up to very insignificant errors. Additional voltage sensitive applications include implantable medical devices and wearable medical electronics. These devices constantly take measurements periodically, and their batteries are changed after long time periods. DC-DC converters with compact size are essential to their design, while maintaining accurate supply voltages for accurate biometric measurements. Also, high efficiency is essential to maximize battery life. Accordingly, the main criteria for medical electronics are size, efficiency, and minimized output voltage ripples.

1.2 Challenges

Since portable devices have dominated the consumer electronics industry, the demand for technologies fitting their criteria has increased. As mentioned earlier, modern day applications have high requirements, in terms of efficiency and size in particular. Therefore, DC-DC converters have a set of defined metrics based on which they are measured.

First, there is the voltage range and conversion ratio, which determines the range of operation of the DC-DC converter and the ratio between the input and output voltages. Secondly, the rated load current range determines if the converter can function at high load or low load applications. Also, the total converter area and power density both factor in the converter selection criteria for different applications. Other criteria, such as the operating conditions, allow matching a defined converter to specific applications, in order to obtain maximized performance and optimized design. These conditions include maximum output voltage ripples, frequency of operation, thermal management, and reliability [10]. Other important aspects for converters include PCB profile (height) of components on board, where the limitation is usually the inductor size, if the circuit requires an inductor [11]. These factors determine the capability of integrating the converter and its potential applications.

This creates an important metric for DC-DC converters, which is labeled the total converter area. This area takes into account the PCB height, and it is always preferable to decrease the height in order to fit power supplies in smaller, more compact devices. For instance, handheld devices are constantly getting smaller in size with the sacrifice being shorter lasting power supplies. This occurs because decreasing the inductor size significantly affects overall efficiency in a traditional buck converter, which is the most commonly used DC-DC converter in the industry.

Not only is converter area important for decreasing the device size, it is important to be able to integrate multiple converters instead of just one on a board. Many devices require different voltages for different modules on the same PCB. This necessitates multiple, DC-DC converters. This also applies to some chips, which require a similar concept labeled distributed, on-chip DC-DC converters. Optimizing a distributed power delivery network requires optimizing the number of converters, the capacitance of each converter, and the design layout [12]. Distributed on-chip DC-DC converters also give a boost to the efficiency by reducing IR losses in the interconnects. It has been proven that a reduction in the IR drop by 74% could be achieved using distributed DC-DC converters compared to lumped designs [13]. This concept can be extended to higher power converters that are found on PCBs. However, implementing them can

be challenging if each converter takes up a considerable area. The alternative becomes using a Switched-Capacitor DC-DC converter, which are generally limited by their low efficiency. Hence, area reduction of the more common and efficient converter, the Buck Converter, becomes necessary. The Buck converter's area limitation results from the use of a large inductor with a high quality factor, which is complicated to implement on-chip with high efficiency. Consequently, optimizing the Buck converter design promises better integration without a large compromise in efficiency.

1.3 Approach

First, the traditional DC-DC converters found in the industry and literature are explained and analyzed. According to the analysis, a hybrid converter topology that combines the advantages of common switched capacitor voltage regulators (SCVR) and Buck converters becomes necessary to achieve higher performance with a reduction in size. The loss models of common converters are each analyzed, and the main sources of loss are targeted and eliminated, therefore resulting in efficient converters by using smaller inductors. After finding a suitable design, it is then implemented and tested against the industry gold standard in order to prove its advantages. The targeted applications are portable, handheld devices, but the concept can be extended to other applications including on-chip implementations.

1.4 Scope of Work

Analyzing the literature is necessary before determining the design methodology and techniques. First, a background on voltage regulators in general is presented. The more common types of regulators are introduced and explained in detail. Next, their loss models are analyzed for optimization. Then, a comparison between the advantages and disadvantages of these converters is presented. This allows their limitations to be addressed and an improved topology that solves the problems faced by traditional converters can be developed. Afterwards, the hybrid converter topology and the regulation techniques for it are introduced and discussed. Then, the PCB implementation process of the hybrid converter is described. Finally, the results are shown

and discussed, followed by a conclusion of the research findings and their impact on the power electronics industry.

Chapter 2

BACKGROUND

2.1 Introduction to Voltage Regulators

Various types of voltage regulators (VR) exist in the literature. However, two main types dominate the industry: linear regulators, also called Low-Dropout Regulators (LDR), and switched regulators.

Linear regulators consist of resistive elements and operate by dissipating some of the input power in order to produce a reduced output voltage. These regulators suffer from very limited efficiency, which is constrained by the conversion ratio. Due to the high power dissipation in the LDR circuitry, thermal management requirements are important for protecting the regulator from damage. Yet, linear regulators offer very simple circuitry and relatively small area, making them appealing for compact designs with flexible power requirements.

Switched regulators function by transferring charge discontinuously in order to provide a decreased voltage at the output. Switching regulators are composed of an active switching element and a passive charging element. Switching regulators offer much higher efficiencies than linear regulators, with the cost being area and complexity.

The two common topologies of switched regulators are Switched-Capacitor voltage regulators (SCVRs) and the Buck converter. Both converters use switching elements but differ in the charge storing element being used. The SCVR uses capacitors to transfer charge from the input to the output, while the Buck converter uses an inductor to perform the voltage conversion. Each one of the converters has advantages over the other in terms of efficiency, area, and complexity, making them suitable for different applications.

For any converter, there exists a regulation stage, or a control stage, which is responsible for maintaining a steady output voltage that is regulated from the input voltage. It is required that the output voltage tracks a certain reference voltage that is assumed to be lower than the input voltage, assuming a step-down converter. The most common control techniques can be used with either SCVRs or Buck converters; therefore, both would be applicable to hybrid converters. Hence, control mechanisms for all converter types need to be explored to optimize both the conversion and control stages.

2.2 Switched-Capacitor Converters

SCVRs use charge transfer capacitors to move charge from the input to the output, while varying the connections between the capacitors in order to produce a different voltage at the output. The SCVR usually operates in two phases, where some of the switches connecting the capacitors are on at one phase, with the rest being on at the second (or more) phase. Figure 2.1 shows an example of a switched-capacitor converter operating in two phases, with some switches turning on during the first phase, with the other switches turning on during the second phase. In the first phase, the capacitors are connected in series to have the input voltage divided on the capacitors, and they are then connected in parallel during the second phase, in order to obtain a decreased output voltage with an increased output current (which maintains a high efficiency). SCVR applications include wireless sensor node converters, energy harvesters, ultracompact energy storage conversion [14]. The SCVR can be optimized by finding limits for the output resistance and efficiency, which allows comparison of SC converters, for more accurate topology selection methods [15].

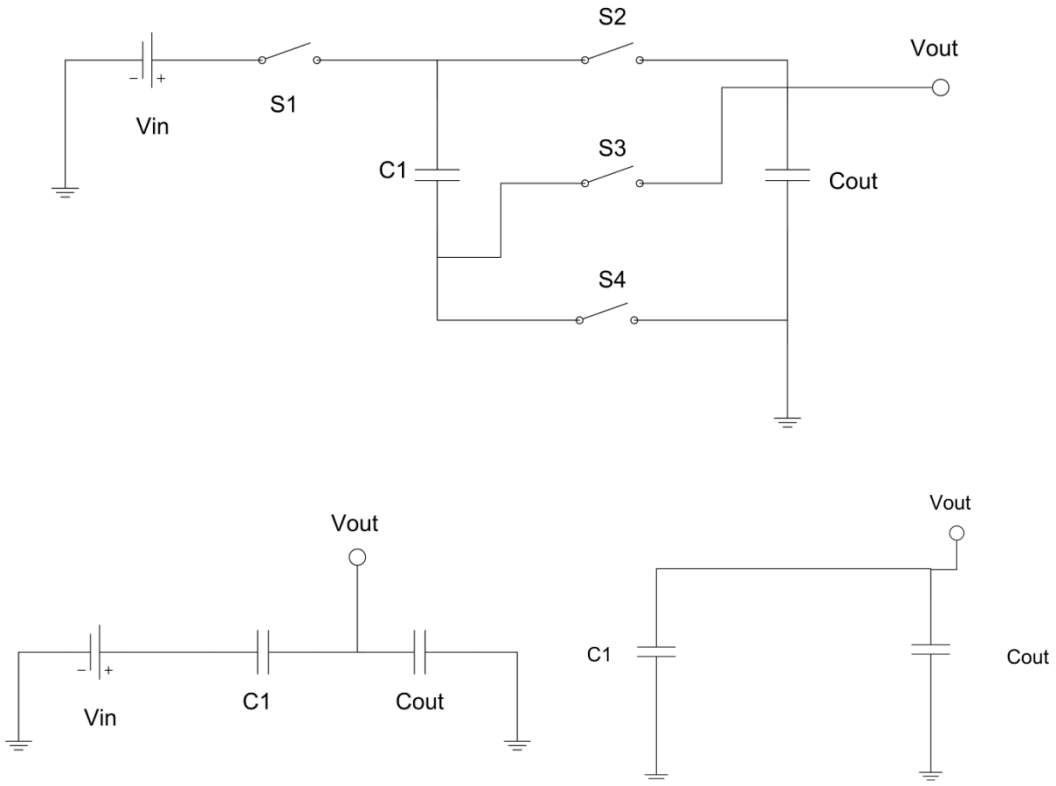

Figure 2.1. Switched-Capacitor voltage regulator operating in two phases (top), where switches 1, 3 are on in phase 1 (bottom left), and switches 2, 4 on in phase 2 (bottom right).

2.2.1 SCVR Control Mechanisms

First, the control methods in SCVRs range from frequency modulation, topology control, to digital capacitance modulation, and switch modulation. Equation (2.1) shows the relationship between the output resistance of the converter, *Rout*, and many factors that come into play when optimizing the efficiency, and could also be used to change the conversion ratio [14]. It is shown that the output resistance is proportional to the on-resistance of the switches R_{on}, and inversely proportional to the switching frequency F_{SW}, flying capacitance C_i, and the duty cycle D_i, which are all flexible for optimization and modulation. Since the output resistance is inversely proportional to the output voltage, virtually unlimited combinations could be implemented to obtain ultradynamic voltage scaling (UDVS).

$$\boldsymbol{R_{out}} \propto \frac{\mathbf{1}}{\boldsymbol{C_i F_{sw}}} + \mathbf{2}\frac{\boldsymbol{R_{on}}}{\boldsymbol{D_i}} \tag{2.1}$$

2.2.1.1 SCVR Topology Control

The clear technique of changing conversion ratios on a SCVR is changing the topology by changing the switching to make different combinations of the capacitors in different phases. This is implemented heavily in the literature due to its efficiency and the minimalistic additional control circuitry. For instance, a circuit is implemented in [4] where 5 topologies are available for controlling 5 different conversion ratios. The overhead circuitry is very minimalist, while the output range is increased dramatically. It is shown in Figure 2.2 that several topologies are easily attainable by changing the switch configurations.

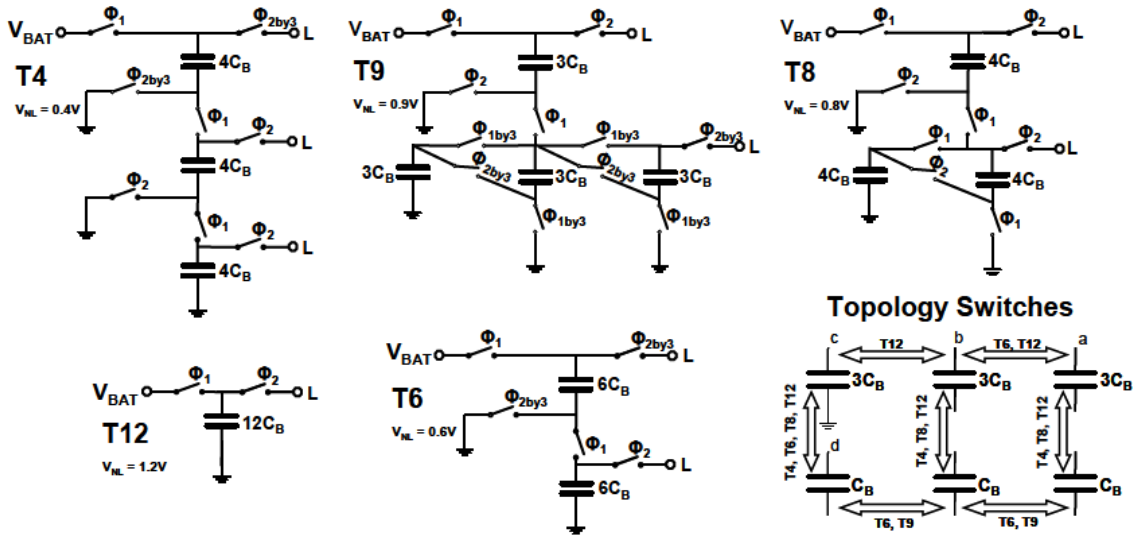

Figure 2.2. Five possible topologies that can be integrated in one SCVR circuit using only 6 capacitors and 13 switches [4].

2.2.1.2 Frequency Modulation

The most efficient form of output regulation for both Buck converters and Switched-Capacitor converters is Pulse Frequency Modulation (PFM), as it changes the operating point of the converter as a whole, without causing significant losses. In the Buck converter, it allows maintaining the same efficiency, while adjusting the frequency according to the load power required, in which the frequency increases as the load current increases. The same implementation is possible for SCVRs; however, it is not only used to regulate the current output with changing loads, but also to change the output voltage (and conversion ratio) on the same

load by decreasing the frequency to provide a smaller output. Frequency modulation has also been referred to as SSL modulation, since it directly enhances or degrades the SSL impedance.

This technique, used in [4], provides more conversion ratios at the expense of the efficiency, since SCVRs are sensitive to producing output voltages that are far from the ideal no-load voltage of the topology in use. This is shown in Figure 2.3 where the efficiency drops as the output voltage ratio moves further from the topology no-load voltage.

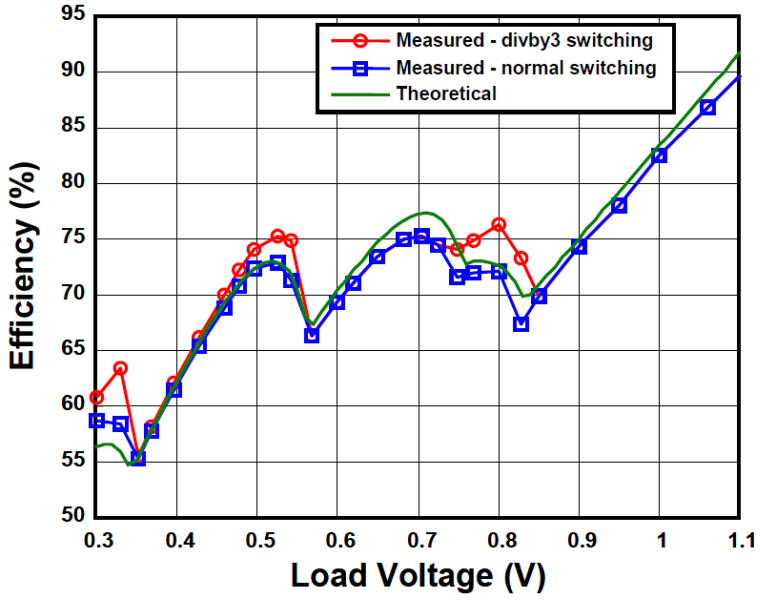

Figure 2.3. Multiple Topology SCVR with efficiency peaks at ideal no-load voltages [4].

2.2.1.3 SCVR Digital Capacitance Modulation

Another method of changing the voltage conversion ratio is varying the flying capacitance value, which allows more charge to be transferred, therefore having a small but sometimes useful effect on output voltage. Yet, the main use of capacitance modulation has been to achieve regulated voltages over changes in load current, which is shown in [16]. Modifying the flying capacitance value is done by adding a series of switches and smaller capacitors, and varying the connections between the capacitors in order to make them in series or parallel. This is done in Figure 2.4, in which different switch combinations provide different values for the flying capacitance.

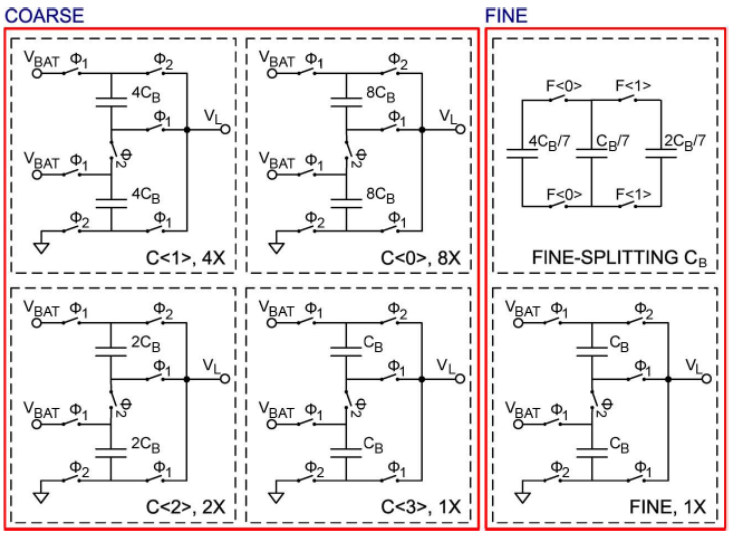

Figure 2.4. Capacitance Modulation Circuit using limited number of capacitors for multiple flying capacitance value based on input vectors [16].

Digital capacitance modulation is preferred to regulate output voltage over load changes due to its resilience to switching noise, which is an issue with Pulse Frequency Modulation (PFM). While PFM is a stable technique of voltage regulation with minimal losses, changing the frequency with load current changes produces varying switching noise in the input and output and is challenging to control. It is shown in Figure 2.5 that digital capacitance modulation provides smooth regulation over different load currents using many capacitance values. Yet, the disadvantage remains to be its overhead circuitry, since the control mechanism is more complex to implement, and the addition of more capacitors and switches, which inevitably has a drastic effect on the efficiency.

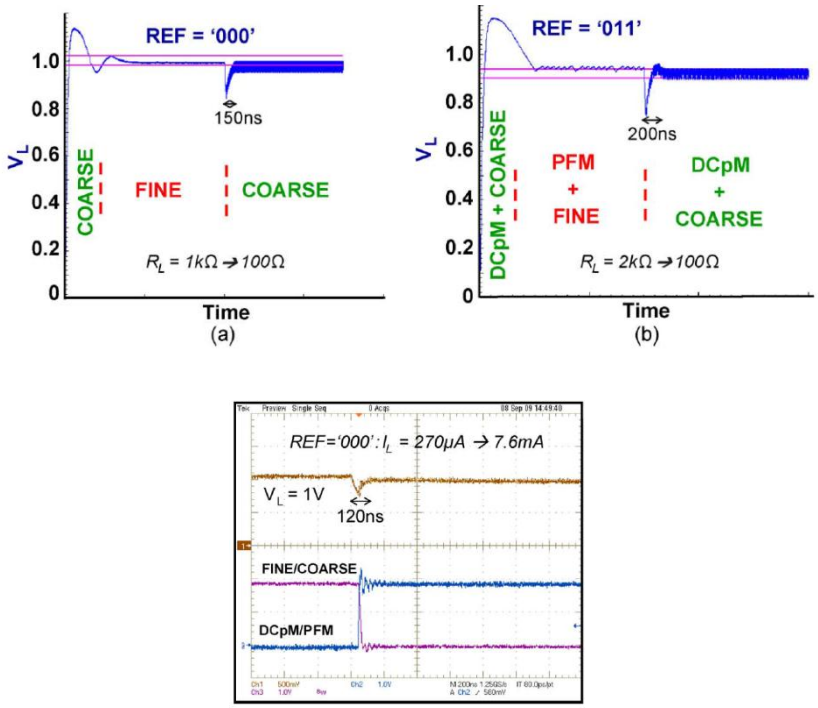

Figure 2.5. Capacitance modulation output voltage change due to reference change [16].

2.2.1.4 SCVR Switch Modulation

Switch size is modulated by increasing the width of the switch in order to decrease the on-resistance, at the expense of increasing the gate capacitance. This produces an improvement in conduction losses, by minimizing the Metal-Oxide Silicon Field-Effect Transistors (MOSFET) R_{dson} while increasing the switching losses, which are directly affected by the switch gate capacitance. It requires very careful optimization to find the most efficient switch size for a particular converter based on the conversion ratio and the load current.

As a result, switch size modulation is not a very common mode of voltage regulation, due to its complexity as well as inefficiency in some aspects. That is mainly true for off-chip applications, while on-chip implementations have proved slight improvement over unmodulated switches [14] [16].

2.2.2 Switched-Capacitor Converter Loss Model

The SCVR is characterized by having more components than a buck converter, and is therefore dominated by parasitic losses due to resistances and capacitances. A SCVR with

multiple topologies also suffers from complexity in modeling the different configurations of the switches and capacitors, and requires simplified modeling for accuracy. Complexity also results from the different control circuits, clock sources, and topology controllers [12].

Yet, the main sources of losses are consistent in all switched-capacitor converters, consisting of conduction losses, switching losses, parasitic losses, and regulation losses.

2.2.2.1 Conduction Losses

Conduction losses result from charging a capacitor through a switch that has a known on-resistance [4]. The power is lost in the switches while charging the flying capacitors can be expressed by Equation (2.2), where M_{sw} is a constant determined by converter topology, I_{out} is total current delivered by converter, R_{on} is switch resistance per unit width, and W_{sw} is switch width [12].

$$\boldsymbol{P_{cond} = M_{sw} \cdot \frac{{I_{out}}^2}{N_{phase}} \cdot \frac{R_{on}}{W_{sw}}} \tag{2.2}$$

It is shown that energy is lost through the switches, but the conduction losses also include energy lost on the capacitor equivalent series resistance (ESR) during each charge transfer to or from a capacitor. The energy loss, however, is minimized by having smaller AC voltage components, which is done by minimizing the voltage ripples and maximum voltage swing [15]. Conduction losses are also affected by the operating frequency, where low frequency results in high peak current which decreases efficiency [10].

2.2.2.2 Switching Loss (Gate Drive Loss)

Gate drive loss, or switching loss, is the energy lost through switching the gate capacitances of the charge-transfer switches at every phase. These losses can be expressed by Equation (2.3), where n expresses the number of switches, C_{GSw} is the gate capacitance per switch, V_{dd} is the supply voltage, and F_{sw} is the switching frequency [17].

$$\boldsymbol{P_{sw} = n \cdot \left(\frac{1}{2}\right) \cdot C_{GSw} \cdot {V_{dd}}^2 \cdot F_{sw}} \tag{2.3}$$

Another expression for switching loss can be derived for on-chip applications, where the switches can be designed differently. In Equation (2.4), N_{phase} represents the number of phases, n is the number of switches, F_{sw} is the switching frequency, C_{GSw} is the gate capacitance per unit width, W_{sw} is the width of the switch, and V_{dd} being the supply voltage [12].

$$\boldsymbol{P_{sw} = N_{phase}.n.F_{sw}.(C_{GSw}.W_{sw}).V_{dd}^{2}} \tag{2.4}$$

In this case, it can be seen that the switching losses are dependent on gate capacitance relative to the switch width, which affects both switch resistance and gate capacitance. It is also noted that the effect of the supply voltage is quadratic, giving it significant weight when optimizing. Also, the switching frequency affects both switching power and root mean square resistive conduction loss due to ripple current [18].

2.2.2.3 Parasitic Losses

Parasitic losses comprise mainly of bottom plate capacitance, resulting from use of on-chip capacitors which create a capacitance between the plate and the ground bottom plate. The losses occur due to the charging of the bottom plate parasitic capacitance of the charge transfer capacitors every charge cycle [4].

These parasitics are very dominant in on-chip applications, but do not apply to PCB or off-chip converters. Yet, the effects of bottom plate capacitance result in 20% more parasitics at the bottom plate, making the efficiency suffer significantly [8]. It can be observed from Equation (2.5) that parasitic losses are affected linearly by the topology M_p, the switching frequency F_{sw}, the bottom plate switching capacitance C_{GSw}, and the voltage swing on the capacitor V_{dd} [12].

$$\boldsymbol{P_{para} = M_p.F_{sw}.C_{GSw}.V_{dd}^{2}} \tag{2.5}$$

2.2.2.4 Regulation Losses

Regulation losses result from several factors, including the difference between the no-load voltage and the loaded voltage. This loss is one of the main limitations to the efficiency in SCVRs. The relationship between energy from the battery to the energy delivered to the load is expressed in Equation (2.6), where E_L is the energy delivered to the load, E_B is the energy

transferred from the battery, V_{NL} is the no-load voltage, and ΔV is the deviation of the output voltage from the ideal no-load voltage [4].

$$\boldsymbol{E_L = E_B . \frac{V_{NL} - \Delta V}{V_{NL}}} \tag{2.6}$$

Control circuit power losses are also of concern when delivering ultra-low power levels. There are two components in control power losses, switching and leakage. The switching losses are also referred to as dynamic power losses while the leakage is referred to as static power losses.

2.2.3 Other SCVR Loss Models

One loss model that has become very common when analyzing SCVRs is the one proposed by Seeman, where two limits are described that model the losses depending on the frequency of operation. The two limits, labeled the Slow Switching Limit (SSL) and the Fast Switching Limit (FSL) are characterized by one type of power loss dominating each limit. The low frequency output impedance (Slow switching limit impedance) increases with decreasing switching frequency, which limits the efficiency. It sets the maximum converter power and determines open-loop load regulation properties [19]. The fast switching limit impedance, however, is dominated by the switch on-resistance, interconnect parasitic resistances, capacitor/inductor ESR, and is frequency independent.

The main assumption of this method is two-phase converters; however, it can be applied to multi-phase converters.

2.2.3.1 Slow Switching Limit

The charge flow per period (average current flow) defines the output impedance. The R_{SSL} is inversely proportional to capacitor size and switching frequency. It can be expressed in terms of capacitor loss, in which the sum of the energy lost through the capacitors is equal to the calculated loss associated with the output impedance for a given load.

2.2.3.2 Fast Switching Limit

The other asymptotic limit is the FSL, where conduction loss dominates due to resistive elements. Capacitors don't reach equilibrium due to resistive losses. The FSL is characterized by the assumption of constant current flow between capacitors. The current in the switches increases with charge increase and with increasing the switching frequency. The $R_{FSL}$is directly related to the on-resistance of the switches and the ESR of the components.

2.2.3.3 Model Limitations

The main limitation to charge sharing losses dominating SSL is that the model assumes constant output voltage due to the existence of an output capacitance. However, if variable output is assumed, much higher efficiency could be allowed [20].

It is shown that the SSL is independent of the switch resistances and represents the summation of CdV^2 over each capacitor in the converter where dV is the voltage swing on each capacitor. However, this SSL loss does not examine the case when the load is fully resistive (ideal load), where the output resistance is simply the switch resistance. As the switch resistance approaches 0, the losses are mathematically eliminated; this contradicts the concept that SSL resistance is independent of switch resistance.

As a result, it can be inferred that if the output voltage is not assumed constant, higher efficiency can be reached, but with increased output voltage ripples. It can be found from Equation (2.7) that increasing the output voltage ripples r_{output} increases efficiency by decreasing the output resistance.

$$\boldsymbol{R_{output} = R_{FSL} + \left(1 - \frac{r_{output}}{r_{max}}\right).R_{SSL}} \tag{2.7}$$

This means that as output ripples approach the maximum ripples, the R_{SSL} decreases significantly and could be eliminated. On the other hand, at high values of load capacitance, all ripples disappear and the losses saturate to exactly the SSL specified by Seeman.

2.2.4 Benefits and Drawbacks of SCVRs

The main advantage to using SCVRs is their ease of integrability when it comes to on-chip applications, since they do not use inductors, which are generally more complex in on-chip applications. This allows higher integration capability at a relatively small area footprint, which is dominated by the capacitors. Techniques to design more area efficient capacitors using multiple layer parallel plates can be used in order to further reduce the effective area of SCVRs, and result in better overall integrability.

Yet, the shortcomings of traditional SCVRs lie in their inefficient power conversion, with their parasitics having a significant effect due to the charging and discharging losses. Traditional SCVRs also include extra control overhead, which generates high switching losses since there are generally many switches necessary for driving in order to obtain several output voltages.

2.2.5 Applications of SCVRs

SCVRs are most commonly found in on-chip applications due to their relatively simple integrability. They are also implemented in high voltage up-conversion in very specific automobile applications, where the inductor size requirements for an inductor-based converter would be too high, and a SCVR would be a more area efficient design. Nevertheless, SCVRs dominate on-chip DC-DC converters since new enabling technologies have allowed higher quality factor on-chip capacitors, which lead to better efficiencies, as opposed to inductor-based converters which are limited by low quality factor on-chip inductances.

2.3 Buck Converter

The Buck converter, however, is an inductor-based DC-DC converter. It is more common for off-chip applications because it provides smaller overhead circuitry and lower control circuit power. It generally provides much higher efficiency than a SCVR, with the cost being the large area of the inductor [8]. Buck converters operate by alternating between two phases, one where the input voltage is connected directly to the load through an inductor, and the second phase where the circuit is closed with only the inductor in series with the load, as shown in Figure 2.6. During the first phase, the inductor is charged with current which is discharged in the second phase. The active switching element connecting the ground to the inductor which is turned on in

the second phase can be composed of a diode or a MOSFET transistor. Diodes have been used for simplicity in driving the signal, as well as for blocking any excess charge in the output capacitor from flowing back through the inductor at low load currents. Also, MOSFETs have been used in order to minimize the voltage drop caused by the high threshold voltage of the diodes (and the high on-resistance). Using a switch also allows higher efficiency, with the drawbacks being more complex circuitry, inefficiency at low load currents, and increased power lost in the control circuit. Instead of requiring a single clock source to drive the diode-based buck converter, a MOSFET-based buck converter requires two non-overlapping clock sources, as well as customized controllers to prevent current flowing from the output capacitor back through the inductor.

Depending on the load current, the Buck converter has two modes of operation: Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). In CCM, the voltage conversion ratio of the buck converter is equal to the duty cycle of the controller. As the duty cycle decreases, lower conversion ratios are attainable but at decreased efficiency. In the DCM mode of operation, the conversion ratio depends on the load, which means that the duty cycle affects the conversion ratio nonlinearly [11]. During DCM, losses caused by reflected current degrade the overall efficiency.

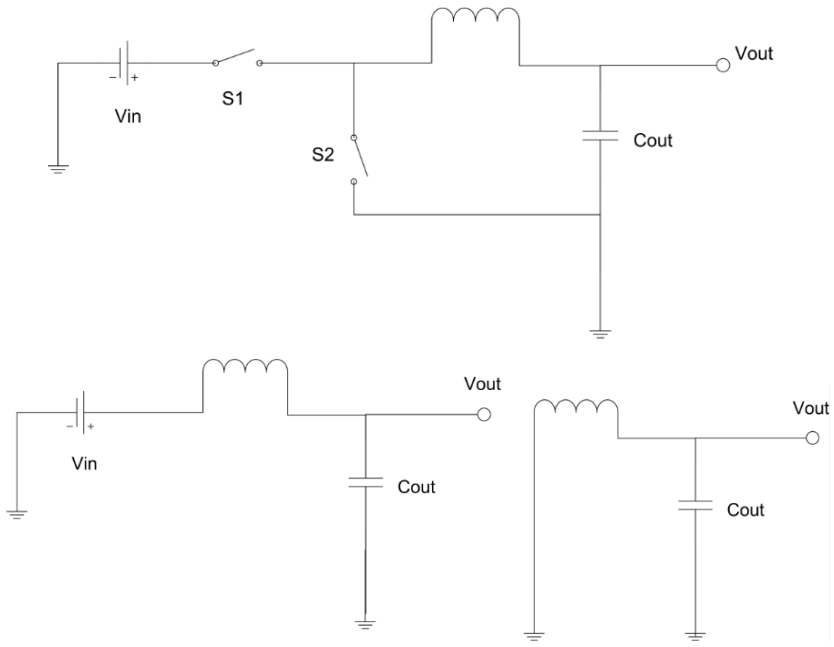

Figure 2.6. Conventional buck converter (top) operating in two phases, phase 1 (bottom left) and phase 2 (bottom right).

Several techniques to optimize the Buck converter exist, which aim to achieve higher performance by implementing small modifications to the existing design. For instance, one method aimed at applications with high currents and low voltages implements a synchronous MOSFET as a replacement for the diode found in regular buck converters. This aims to significantly reduce conduction losses, as MOSFETs have lower resistance than diodes with a high forward voltage. The MOSFETs in the bottom and top switches can then be driven using simple MOSFET drivers [21].

2.3.1 Control Mechanisms

Buck converters are regulated by control methods such as duty cycle modulation and frequency modulation. Each of the mentioned control techniques is described in further detail in the following sections.

2.3.1.1 Buck Duty Cycle Modulation

Buck converters generally dominate duty cycle modulation since it is the main technique used in most Buck converters. Changing the duty cycle of the input voltage with respect to the ground voltage allows dynamic voltages and conversion ratios. This technique allows very high efficiency to be maintained over all voltage conversion ratios, assuming low load current. Varying the duty cycle allows variation of the output voltage while maintaining the same output signal form and frequency, which minimizes control circuit complexity, making it a more favorable control mechanism. However, there are also some limitations to the control signal's simplicity that need to be addressed.

2.3.1.2 Dead-time

A crucial factor in voltage regulator control circuits is the dead-time algorithm used. Dead-time algorithm circuits prevent two switches from overlapping when they should not, which causes current spikes due to short circuit between the supply and the ground. This is done by providing a small period of time between switching two switches, instead of switching them both simultaneously. Without deadtime, some cases consist of the control signal containing non-overlapping signals, while the MOSFET drivers would have some variable delay, which would be the main cause of the short-circuit current spikes. In that case, dead-time compensation is

required to avoid the detrimental effects to the efficiency. Figure 2.7 shows the effect of dead-time elimination on current spikes, and how it improves the efficiency.

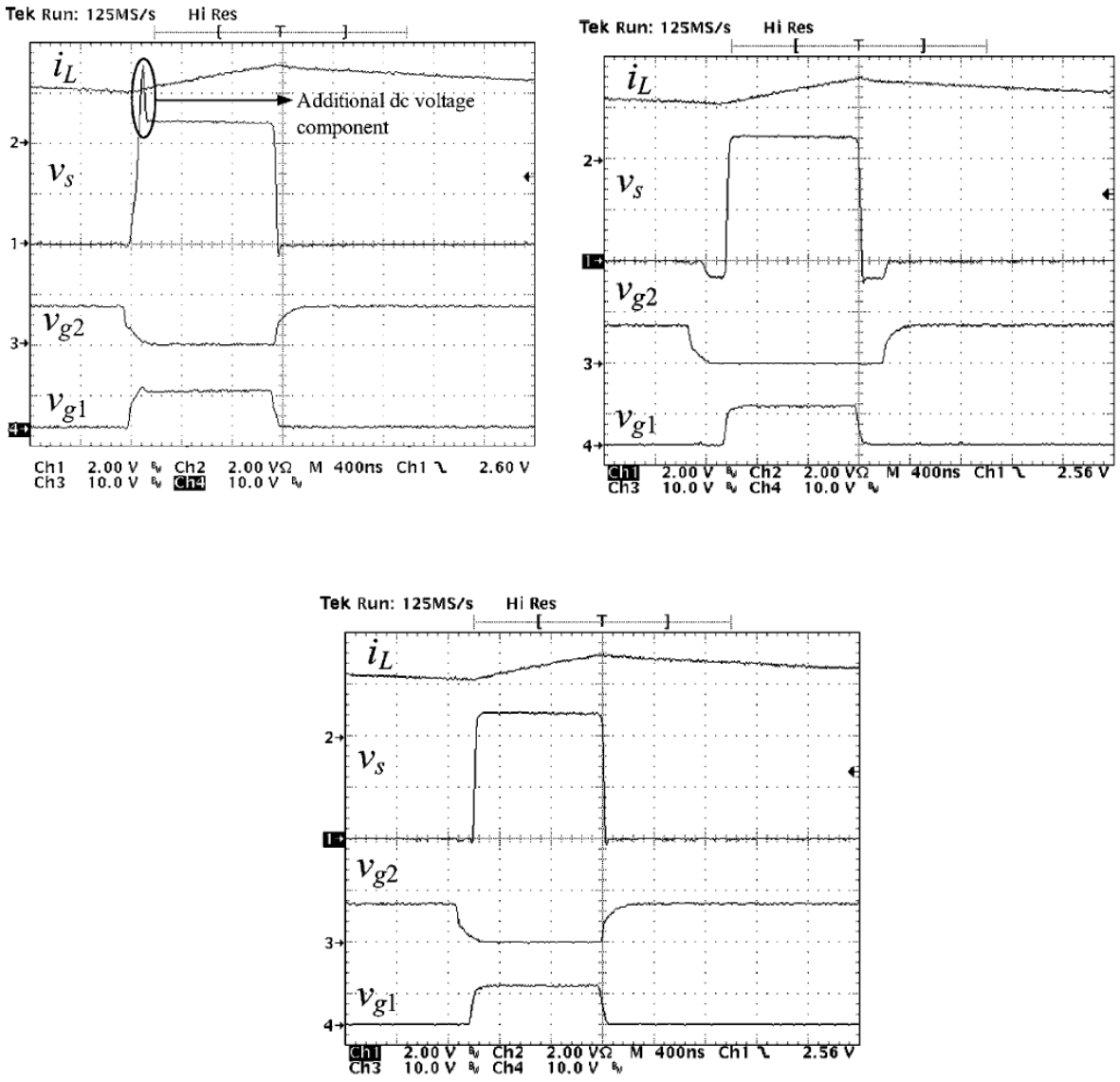

Figure 2.7. Insufficient deadtime added to signals (top left), excessive deadtime added to signals (top right), optimized deadtime added to signals (bottom) [22].

Dead-time algorithms have been shown to improve efficiency by up to 12% in experimental prototypes [22]. Yet, increasing the dead-time between signals is only useful until the efficiency saturates, and increasing the dead-time further than that point results in decreased efficiency if the time is too high. As a result, dead-time is measured or analyzed based on

knowledge of the control signal variation, the MOSFET driver delay variations, and the cycle period.

2.3.2 Buck Converter Loss Model

As for the Buck converter, the loss model includes much less components due to decreased complexity and decreased number of capacitors and switches. This allows reduced parasitics, allowing higher efficiency with the cost being the addition of a high quality factor inductor, which limits metrics other than the efficiency. Yet, some sources of losses remain the same also for the Buck converter, such as the conduction losses caused by the switch resistances and inductor ESR, the switching losses (gate drive losses) caused by the driving the switches, and the control circuitry losses.

In high load currents, power losses in a buck converter are dominated by conduction losses, where I_{load} is high enough to cause major losses in the parasitic resistances [23]. In moderate loads, however, the losses are dominated by the VI overlap and the current ripple induced conduction losses. This is generally the dominant source of loss in most buck converters. At very light loads, the power losses are dominated by gate drive losses, also called switching losses.

Another model suggested in [18] is that the output voltage of a Buck Converter is bound by Equation (2.8), where the duty cycle D, input voltage V_{in}, load resistance R_{load}, switch on-resistance R_{on}, and inductor parasitic resistance R_{ind}, are all significant.

$$\boldsymbol{V_{out-DC} = D.V_{in}.\frac{R_{load}}{R_{load}+R_{ind}+R_{on}}} \tag{2.8}$$

As a result, these parasitics and components are necessary for proper analysis and design for buck converters in order to accurately predict the output voltage. Yet, the Buck Output Voltage Equation assumes continuous mode operation using a synchronous rectifier that does not include a diode.

For further optimization, it is clear from Equation (2.9) that the ripple current, ΔI, is proportional to voltage swing before the inductor V_{swing}, and inversely proportional to the switching frequency f_{sw} and the inductance L [18].

$$\Delta \boldsymbol{I} = \frac{\boldsymbol{V_{swing}}.\boldsymbol{D}.(\boldsymbol{1}-\boldsymbol{D})}{\boldsymbol{f_{sw}}.\boldsymbol{L}} \tag{2.9}$$

Therefore, in order to decrease the ripple currents, and in turn increase the efficiency, it is necessary to decrease the voltage swing before the inductor. That is possible by using switched-capacitor circuits to change the output level between two topologies. A hybrid topology would also combine the advantages of both the SCVR and the Buck Converter.

2.3.3 Benefits and Drawbacks of Buck Converters

The buck converter has several advantages over the traditional SCVR, and of course some limitations. First, the buck converter is able to achieve much higher efficiencies, due to its simple design and control overhead circuitry. It is also relatively simple to implement because its components are mostly accessible. However, this comes with the limitations of its component size, due to the large inductor needed for obtaining high conversion efficiency. As it is discussed earlier, obtaining high conversion efficiency requires high switching frequency, a large inductor, and minimized voltage swing. The only factor that cannot be manipulated by traditional buck converters is the voltage swing, which constitutes a significant limitation.

2.3.4 Applications of Buck Converters

The buck converter's simple design and loss model have proven useful, as it is dominating the off-chip DC-DC converter industry. The high efficiency obtained with minimal overhead makes its advantages appealing for use in power electronics applications such as power supplies in most, if not all, mobile and portable devices.

Buck converters can be found in a majority of battery powered devices, since power conversion efficiency is a key criterion for power supply units in order to maximize battery life. They are dominant due to their simplicity in implementation with minimal control, since a square wave can be used to drive the converter and achieve very high efficiency, with the variation in output voltage being dependent on the duty cycle. Accordingly, the simplest DC-DC converter available for power supplies with high performance requirements is the buck converter, with its limitations being its significantly large area when compared to other converters.

2.4 Traditional Converters Comparison

A comparison is therefore necessary to evaluate the relative benefits of each type of converter and how it surpasses the performance of the other converter. This also clarifies the criteria for evaluation, and how an improved topology for future DC-DC converters is necessary for the improvement of the power electronics industry. A concise comparison of the key features found in both converters and how they differ is found in Table 2.1.

Table 2.1. Performance comparison between traditional SCVRs and Buck converters

Criterion	Switched Capacitor Converters	Buck Converters
Maximum Efficiency	Limited	High
Area Requirements	Low	High
Integrability	Simple	Complex
Control Overhead	High	Low
Output Voltage Ripples	Low	High

2.5 Hybrid Converters

Both the SCVR and buck converters suffer from limitations in their loss models that force designers to seek a more advanced hybrid design that avoids their limitations and combines the advantages of each converter.

The main advantage of the SCVR is its ability to be integrated easily on-chip, with very small area. It also provides flexibility in conversion ratio by switching between topologies, making it a dynamic voltage regulator. However, it suffers from limited efficiency and significant parasitics. The Buck converter, however, is very efficient with very minimal overhead circuitry. However, it requires large area for the high Q inductor and suffers from large voltage ripples caused by the high current ripples. The high integrability, combined with high efficiency, is possible by combining both topologies into a hybrid.

2.5.1 Hybrid Converter Topologies

Despite the fact that a hybrid combining the integrability and small voltage ripples of SCVRs, and the high efficiency of Buck Converters seems like a far-fetched possibility, it is possible to combine two converter stages to obtain relatively important advantages from both converters while eliminating most disadvantages.

A hybrid converter composed of a switched-capacitor in the first stage coupled with a low pass filter in the second stage has been proposed in [24] that aims to eliminate the SSL output impedance described by Seeman, as well as allow several other benefits. A 3-Level Buck converter was also introduced in [25] that combines a capacitor with a buck converter to optimize the efficiency by decreasing the voltage ripples at the inductive stage. The result is a reduced inductor size, which minimizes the total area consumed by the converter compared to a traditional buck converter, as well as the high efficiency associated with buck converters.

If the inductor current ripples are very small, the multi-level converter has up to multiple times higher switch conduction losses. However, if inductor current ripples are more significant (in low voltage applications) the switch conduction loss in the multi-level converter can be similar to or less than that of a standard buck converter.

The 3-Level Buck, shown in Figure 2.8, also allows decreased voltage swing, which increases efficiency at the expense of control circuit complexity and very few additional components. The first stage output voltage is shown in Figure 2.9 to highlight the decreased voltage ripples, which are averaged by the inductor to provide a smoother, more efficient output. The efficiency of the ideal VR is inversely related to the output voltage ripple [17]. Therefore, decreasing the output ripples allows higher efficiency.

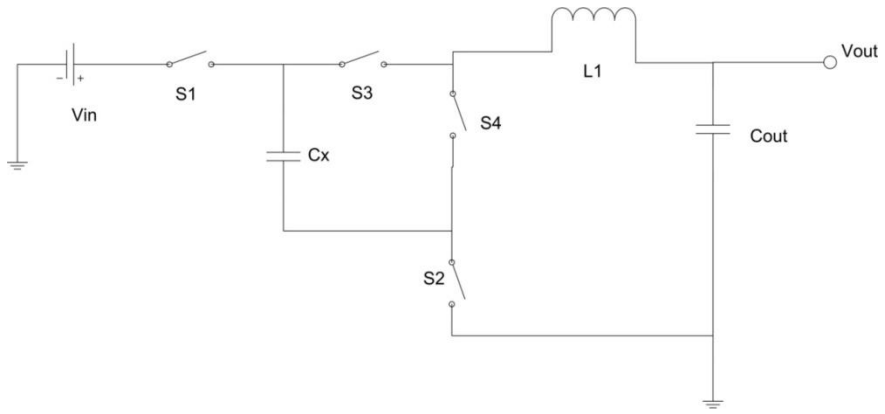

Figure 2.8. 3-Level Buck Converter.

The first stage operates by utilizing the switches and the capacitor to output a voltage that is a fraction of the Buck output voltage, while combining it with the full voltage output, in order to reduce the ripples. The second stage eliminates the noise, providing a suitable output voltage, while maintaining high efficiency. Results have indicated significant improvements in output voltage ripples, as is shown in the comparison in performance in Figure 2.9 [25].

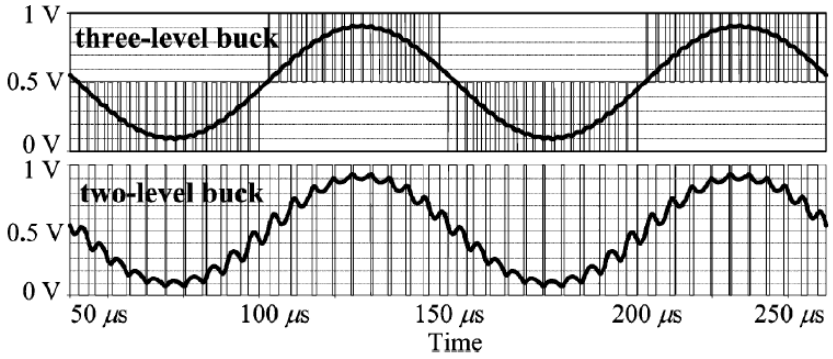

Figure 2.9. 3-Level Buck Converter Output ripples vs. Conventional Buck output ripples [25].

An extended concept that would be implemented in hybrid converters is that of the multi-level multi-state hybrid converter, where the output of the switched-capacitor stage alternates between two levels. This requires a switched-capacitor circuit with the ability to output several voltage outputs by changing the configuration, and in return, the conversion ratio [26]. Introducing a series inductor to the SC converter provides adiabatic charging of the energy

transfer capacitors, which eliminates SSL loss. We use small inductors to obtain high conversion efficiency. Overall, this enhances SCVR efficiency by simply adding a low Q inductor [27].

The requirements for such a converter to operate efficiently are that the minimum Q (Quality Factor) for the inductor is 0.5 for optimal operation, and the frequency to exceed a certain damping frequency. Equations (2.10), (2.11), and (2.12) demonstrate the minimum frequency requirements for proper functionality of the hybrid converter [24].

$$\boldsymbol{W_O = \frac{1}{\sqrt{LC}}} \tag{2.10}$$

$$\boldsymbol{W_D = W_O\sqrt{1 - \frac{1}{4Q^2}}} \tag{2.11}$$

$$\boldsymbol{f_{SW} > f_D} \tag{2.12}$$

Operating at a frequency near or below the damping frequency f_D creates a difficulty for the operation of the converter due to the LC time constant being smaller than the period, when proper operation requires that multiple switching periods occur within one LC period to prevent the LC circuit from damping. Therefore, operating properly eliminates the SSL loss for frequencies higher than the damped frequency. This allows functionality in the FSL region at a lower frequency, which results in higher efficiency. Adding the inductor has a similar effect as increasing the flying capacitor size (capacitance), however merely a small inductor is needed for that effect.

The implementation of a control signal could be simply by alternating between two voltages with each voltage level comprising of two or more phases, yet an interesting technique is used in [26] where the 4 phases of each voltage level are interleaved, which provides many benefits including increased frequency at the inductor and reduced current ripples at the output.

2.5.2 Ultradynamic Voltage Regulation

Obtaining a wide range of output voltages for a DC-DC converter is important for a converter that is implemented targeting dynamic voltage scaling applications. This is simply implemented by an LDR or a Buck converter, but the conversion efficiency drops significantly

as the conversion ratio increases. Accordingly, it is important to find a converter that tackles this challenge. A hybrid converter presents a topology that allows a wide range of conversion ratios along with high efficiency throughout that range.

Several techniques can be also used to obtain different conversion ratios based on a reference voltage. It is also possible to track changes in the load current, which cause small changes in the load voltage. For instance, a load-dependent technique is used in [23] to maintain high efficiency over diverse load ranges using mode-hopping. The technique also makes use of hysteretic control, in order to regulate the output voltage while adapting to changes in the current ripples; the result is optimized and minimized conduction and switching losses.

2.5.2.1 Hysteretic Control Limitations

Some limitations apply to the control circuit, such as hysteresis, which significantly affects most of the regulation techniques. Inaccurate hysteresis calculation for frequency or topology modulation could have very detrimental effects on the overall converter efficiency. This could occur due to increased instability, resulting from oscillations between two topologies, or two frequencies. The efficiency would not only decrease, but the voltage ripples at the output would also increase significantly.

Therefore, the solution becomes increasing the hysteretic value enough to prevent oscillations, while at the same time avoiding slow response time. The responsiveness of a converter to slight changes in the reference voltage is an important factor to consider. Hence, it is required for an ultradynamic converter to have minimal response time to changes in the reference voltage, and to changes in the output voltage resulting from different load currents.

2.6 Chapter Summary

Seeing as the conversion efficiency is one of the main metrics of a DC-DC converter, the sources of power loss are of interest to maximize performance. The buck converter and switched-capacitor converter both have very different sources of losses, and are therefore modeled differently. Power losses result from several factors, including device parasitics, control signals, and inherent topology limitations. The comparison presented shows the different advantages each converter has over the other. Yet, a method to achieve all the advantages is

necessary to meet the industry requirements for an efficient, small converter, to keep up with the trend. The hybrid converter has been presented and discussed, with emphasis on its voltage ripple reduction. The 3-Level hybrid buck converter topology is explored, and its advantages are demonstrated. It is proposed that exploration of other hybrid topologies will lead to further optimization of DC-DC converters, and would allow a design that combines the advantages of the traditional converter types.

Chapter 3

DESIGN OF A HIGH POWER 5-LEVEL 8-STATE HYBRID VOLTAGE REGULATOR

3.1 Introduction

The hybrid converter presents a potential for enhancing the existing DC-DC converter topologies by combining their advantages and eliminating their drawbacks. This is possible by eliminating the SSL impedance found in traditional SCVRs or decreasing the voltage ripple at the inductor input of a traditional buck converter; there are two methods of describing the hybrid topology. This results in increased performance, or decreased inductor size for the same efficiency. For high power applications, this reduction in inductor size would be appealing in order to decrease the total device size while maintaining high efficiency, since a small change in the DC-DC converter efficiency has a significant impact on overall device efficiency and power consumption. Therefore, a PCB implementation is necessary to prove that proper functionality of the hybrid converter achieves higher performance while putting restrictions on inductor size, and would result in decreased output voltage ripples. To verify the advantages of using a hybrid topology over a conventional Buck converter, a 5-Level 8-State Hybrid Regulator is analyzed, implemented on a PCB, and measured against a reference Buck Converter and a 3-Level Converter under the same conditions.

3.2 Converter Architecture

The hybrid converter will contain the first stage from a switched-capacitor circuit that provides five output voltages according to the topology in use. The second stage will be an inductive filter followed by an output capacitor to filter out any ripples. The aim is to achieve adiabatic charging which results in SSL impedance loss elimination.

3.2.1 SCVR Topology

Several SCVRs make use of multiple topologies to achieve different conversion ratios. However, the criteria for selection are both simplicity (to minimize losses) and optimal functionality. As Equation (3.1) shows, the maximum efficiency is bound by the ratio between the variation from the output voltage to the ideal no-load voltage [4].

$$\boldsymbol{\eta_{max} = (1 - \frac{\Delta V}{V_{NL}})} \tag{3.1}$$

SCVRs generally limit the maximum efficiency that can be achieved by a certain topology, where the further away the output voltage is from the no-load voltage, V_{NL}, the higher the ΔV, and the smaller the maximum efficiency that can be achieved by this topology. This is a fundamental problem with charge transfer using capacitors and switches only. Therefore, alternative topologies must be used that produce ideal outputs close to the desired output voltage, or utilize another voltage scaling mechanism other than only topology change. Having several output voltages also helps decrease the voltage ripple at the inductive filter stage, since the voltage alternates between two levels that are closer to each other. This reduces the wasted power within the converter, and in return allows higher efficiency [12].

For these reasons, the topology must provide sufficient voltage levels so that conversion ratios are evenly spread out from each other in order to maintain that the maximum efficiency is reached. Yet, the topology to be selected also needs to minimize the number of switches in the path between the input and the output. It should also minimize the number of capacitors to avoid multiple capacitor ESR, which causes increased conduction losses. Minimizing the number of switches also reduces the total switching losses linearly.

As for the number of switched-capacitor stages, it has been found that efficiency can be improved by increasing the number of stages, but this raises the dropout voltage [28]. Such a dropout voltage could be reduced by increasing the switching frequency and the flying capacitance, or by maintaining a duty cycle close to half. However, increasing the number of stages results in increased parasitics, which could be detrimental to the efficiency and voltage ripples in a hybrid topology requiring multiple output voltage levels. Henceforth, a simple,

minimalist topology is required that is capable of providing multiple voltage levels to reduce the voltage ripples while maintaining high efficiency.

As a result, the topology of interest is the Switched-Capacitor with Inductive Filter hybrid found in [26], which offers the desired minimalistic approach, while providing five output voltage levels, as shown in Figure 3.1.

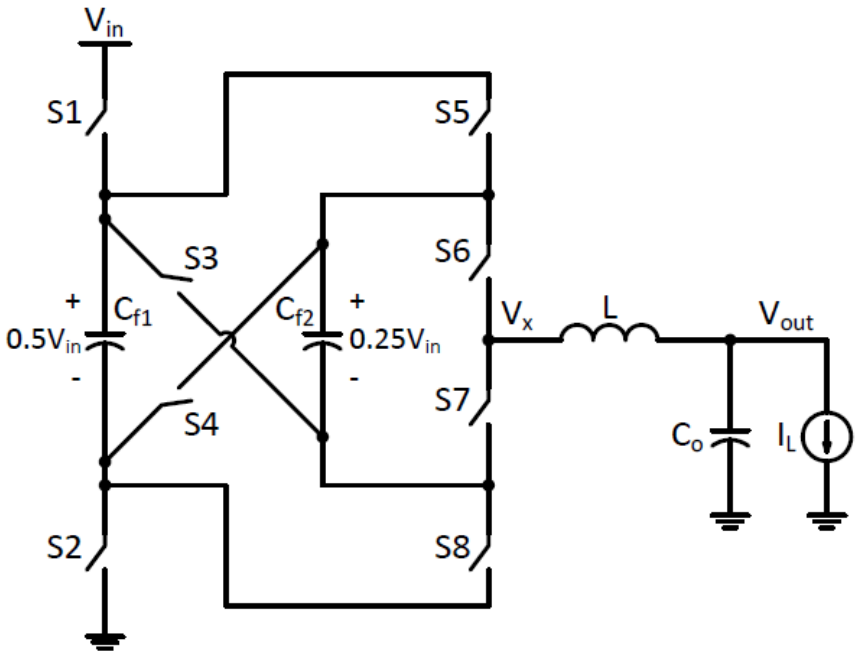

Figure 3.1. Adapted 5-Level Hybrid Converter circuit structure [26].

The circuit consists of two flying capacitors along with eight switches, followed by an inductor and an output capacitor to filter out the AC signal. The two flying capacitors are utilized to provide five voltage levels at the inductor input. The output voltages are *Vin*, *0.75Vin*, *0.5Vin*, *0.25Vin*, *0*. Accordingly, a combination between each two levels can be used to alternate at the inductive filter stage, and produce an output that is an average of both levels, depending on the duty cycle ratio. Assuming that the two flying capacitors are balanced at *0.5Vin* and *0.25Vin*, the five voltage levels can be obtained by one or more configurations of the switches, as shown in Table 3.1. Each configuration of switch input vectors results in certain connections between the capacitors, the input, the ground, and the *Vx* node, where the capacitors would be in the charging

state, discharging state, or floating state. The absolute *Vin* and *0* states are provided by connecting the power supply rails or the ground node to the output directly.

3.2.2 Control Signals

Implementing efficient control signals was necessary to obtain the maximum number of output voltages using the limited number of switches and capacitors. Accordingly, the input vectors controlling which switches would be ON for proper functionality and operation are found in Table 3.1, in which each voltage level requires switching to its relative vectors. To obtain an output voltage that is between two voltage levels, the switch configuration has to complete a cycle of each voltage level's input vectors. For instance, applying an output voltage between *0* and *0.25Vin* would necessitate that the input vector sequence be: <S2 S5 S7>, <S2 S6 S8>, <S1 S4 S7>, <S2 S6 S8>, for the *0.25Vin* output level, followed by <S2 S7 S8> for the *0* output level.

Table 3.1. Switch Configurations providing each Voltage Level

Voltage Level	**Turned On Switches**
Vin	S1 S5 S6
0.75Vin	S1 S5 S7
	S1 S6 S8
	S2 S3 S6
0.5Vin	S1 S7 S8
	S2 S5 S6
0.25Vin	S1 S4 S7
	S2 S6 S8
	S2 S5 S7
0	S2 S7 S8

3.2.2.1 Phase-Interleaving Technique

A technique used in the control signal is that of Phase-Interleaving the signals of a controller [29]. For a particular muti-phase converter, the controller's signals might alternate between more than one group of phases (each one representing a voltage level). In that case, interleaving the phases of each voltage level could be implemented in order to optimize the performance, as is shown in Table 3.2, in the case of the converter topology used in this implementation.

In the case of [26], particularly, phase interleaving provided increased performance through offering increased frequency at the inductor, increased overall stability, and enhanced current ripples.

Table 3.2. Switch Configurations in the Four Operation Regions.

Time slot	First Operation Region				Second Operation Region				Third Operation Region				Fourth Operation Region			
	0.75Vin<Vout<Vin				*0.5Vin<Vout<0.75Vin*				*0.25Vin<Vout<0.5Vin*				*0<Vout<0.25Vin*			
	Vx	ON Switches	Cf1	Cf2	*Vx*	ON Switches	Cf1	Cf2	*Vx*	ON Switches	Cf1	Cf2	*Vx*	ON Switches	Cf1	Cf2
T1	*Vin*	S1 S5 S6	-	-	*0.75Vin*	S1 S5 S7	-	▲	*0.5Vin*	S1 S7 S8	▲	-	*0.25Vin*	S2 S5 S7	▼	▲
T2	*0.75Vin*	S1 S5 S7	-	▲	*0.5Vin*	S2 S5 S6	▼	-	*0.25Vin*	S2 S5 S7	▼	▲	*0*	S2 S7 S8	-	-
T3	*Vin*	S1 S5 S6	-	-	*0.75Vin*	S1 S6 S8	▲	▼	*0.5Vin*	S1 S7 S8	▲	-	*0.25Vin*	S2 S6 S8	-	▼
T4	*0.75Vin*	S1 S8 S6	▲	▼	*0.5Vin*	S2 S5 S6	▼	-	*0.25Vin*	S2 S6 S8	-	▼	*0*	S2 S7 S8	-	-
T5	*Vin*	S1 S5 S6	-	-	*0.75Vin*	S1 S5 S7	-	▲	*0.5Vin*	S2 S5 S6	▼	-	*0.25Vin*	S1 S4 S7	▲	▲
T6	*0.75Vin*	S1 S5 S7	-	▲	*0.5Vin*	S1 S7 S8	▲	-	*0.25Vin*	S1 S4 S7	▲	▲	*0*	S2 S7 S8	-	-
T7	*Vin*	S1 S5 S6	-	-	*0.75Vin*	S2 S3 S6	▼	▼	*0.5Vin*	S2 S5 S6	▼	-	*0.25Vin*	S2 S6 S8	-	▼
T8	*0.75Vin*	S2 S3 S6	▼	▼	*0.5Vin*	S1 S7 S8	▲	-	*0.25Vin*	S2 S6 S8	-	▼	*0*	S2 S7 S8	-	-

The average voltages on the flying capacitors are therefore balanced at *0.5Vin* and *0.25Vin*, which is shown by solving their KVL equations of the configurations providing each

level. Solving these equations for all five configurations allows the circuit to achieve five voltage levels while maintaining maximum efficiency, since all components are used to their full capacity and with minimized charging and discharging of the capacitors. This allows the minimization of the effect of their parasitic losses, since any charging or discharging goes through the capacitor's parasitic equivalent series resistance.

The basic concept of the 5-Level hybrid converter's operation resembles that of a traditional buck converter, in which its normal operation necessitates that the node *Vx* before the inductor switches periodically between two levels; these levels are *0* and *Vin* in the case of a traditional buck converter. Afterwards, the inductor followed by the output capacitor take the weighted average of those two voltage levels, depending on the duty cycle, and generate an output DC voltage. In the case of a 3-Level converter, the two levels are *0* and *0.5Vin* or *0.5Vin* and *Vin*. Accordingly, for the case of a 5-Level converter, the two levels are *0* and *0.25Vin*, *0.25Vin* and *0.5Vin*, *0.5Vin* and *0.75Vin*, and *0.75Vin* and *Vin*. These four operation regions are selected based on where the desired output voltage lies, and this can be considered a form of coarse tuning of the output voltage.

For the fine tuning of the output voltage within an operation region, the relative duration between each two voltage levels can be controlled by varying the duty cycles. Increasing the duty cycle of each level results in a change in the output voltage to be a weighted average of the two levels, with the duty cycle being taken into account, as is shown in Equation (3.2).

$$\boldsymbol{V_{out\ (no-load)} = (D).V_{level\ 1} + (1 - D).V_{level\ 2}} \tag{3.2}$$

This converter topology also satisfies other criteria, since it is important to select the topology that suits the application and utilizes the components best. Some converter topologies use capacitors efficiently while others use switches efficiently, but none are superior in both asymptotes [19]. Converters designed using a capacitor limited process should use a series-parallel topology, which is optimal in the SSL comparison, where all capacitors support the same voltage. Switch limited designs should use the ladder topology, which are optimal in the FSL comparison, where all switches support the same voltage. Therefore, the hybrid topology will optimize between the SSL and FSL, due to the multiple topologies that can be accessed by the SCVR, while having a balance between series and parallel combinations.

3.3 Operating Point

The converter operating point includes the frequency of operation, output load current, the range of duty cycles, the output voltage configurations and conversion ratios, and the target voltage ripples. These factors must be analyzed and simulated before implementations, since they could drastically affect the circuit behavior if not considered in the early design stages.

For the switched-capacitor stage frequency of operation, the requirements are that the frequency is optimized to provide maximum output power while maintaining high efficiency. It must also satisfy the conditions stated in [15] in which the switching period must be higher than the time constant of the LC tank at the output stage in order to maintain that charge/discharge transients be completed within each cycle, where converter efficiency and output resistance reach their best possible limits. However, the efficiency η is maximized when the output resistance R_o is minimized, which is fulfilled by having a small switching period, T_s, as shown in Equations (3.3) and (3.4). That is because an increase in load current for a given switching frequency results in decreased efficiency, and requires increasing the frequency of operation to compensate.

$$\boldsymbol{R_o = \frac{p}{q}.\frac{T_s}{C}} \tag{3.3}$$

$$\boldsymbol{\eta = \frac{1}{1+\frac{R_o}{R}}} \tag{3.4}$$

As a result, an optimum frequency of operation lies between the low frequency required for proper capacitor charge/discharge, and the high frequency required for high SCVR efficiency.

As for the inductive filter frequency requirements, it is shown from Equations (2.10), (2.11), and (2.12) in Chapter 2, that there exists a minimum damping frequency f_D that is obtained from the inductance *L*, output capacitance *C*, and inductor quality factor *Q* [24]. The switching frequency f_{SW} is required to be higher than the damping frequency to ensure proper operation of the inductive filter, creating a third boundary condition for converter frequency optimization.

The second operating point factor is the load current optimization, which depends on several elements including the duty cycle D, voltage ripple V_{ripple}, Inductor Size L, and switching frequency f_{sw}, as shown in Equation (3.5) [18].

$$\frac{\Delta I}{2} = \frac{V_{ripple}.D.(1-D)}{2.f_{sw}.L} \leq I_{out} \tag{3.5}$$

Operating at high load currents results in increased conduction losses due to parasitic resistances. Also, operating at very low currents results in decreased efficiency due to the switching losses dominating the losses. Therefore, optimizing the load current I_{out} using Equation (3.5) is essential to optimal performance. Due to the numerous variables available, some factors such as the frequency and voltages should be identified and then the inductor size, duty cycle, and load current could be optimized by sweeping all possible values.

The minimum inductance for specific components could be derived. The relationship between the minimum inductor size L_{min} and the switching frequency f_{sw}, duty cycle D, and resistances is expressed by Equation (3.6) [18].

$$\frac{L_{min}}{(R_{load}+R_{on}+R_{ind})} = \frac{(1-D)}{2.f_{sw}} \tag{3.6}$$

3.3.1 Operating Voltage

For the operating voltages, the industry standard for portable devices' battery voltage ranges from 3V to 5V. As a result, it is important for a converter whose main purpose is area reduction to operate in that voltage range. The output voltage levels of the switched-capacitor stage become 3V, 2.25V, 1.5V, 0.75V, and 0V for a 3V input, and 5V, 3.75V, 2.5V, 1.25V, and 0V for a 5V input.

In that case, the ripple voltage at the output of the first stage is 0.75V for a 3V input and 1.25V for a 5V input due to the hybrid model. This allows a reduction in voltage ripple by four times, which gives much more flexibility when optimizing the current ripples for different inductor sizes and frequencies.

3.4 Circuit Loss Model

When modeling the dominant losses due to the SCVR in the hybrid converter, the most appropriate loss model to use is the SSL and FSL model [19]. That is due to the fact that the losses are mainly caused by a low frequency of operation, which emphasizes the SSL loss, and reduces the switching losses, which could become a significant problem at low load currents.

It is known from the loss model that obtaining the minimal converter output impedance corresponds to the maximum efficiency for a given delivered power, and also corresponds to maximum power delivery for a given loss. When optimizing over capacitance size or switch size, one should minimize the output impedance.

One should also optimize for the appropriate voltage to be on the capacitors. There are two important voltages for capacitors operating in a SCVR: the working voltage and the rated voltage. The working voltage for a capacitor is the maximum voltage on a capacitor during steady-state converter operation. The working voltage must be less than the rated voltage to avoid damaging the component and should be close to the rated voltage to achieve good utilization of the device. The slow switching limit impedance increases quadratically with increasing rated voltage. Also, the capacitor ripple voltage increases linearly with the rated voltage of the capacitor. For a switch, also, the working voltage is the voltage it blocks during steady-state operation, which is important to be lower than the rated voltage.

3.4.1 SSL and FSL Optimization

The SSL, which dominates at lower frequencies, is calculated using Equation (3.7), where the constant $a_{c,i}$ is topology dependent, and is composed of multiple components, based on the number of phases.

$$\boldsymbol{R_{SSL}} = \sum_{\boldsymbol{i}} \frac{(\boldsymbol{a_{c,i}})^{\boldsymbol{2}}}{\boldsymbol{C_i \cdot f_{sw}}} \tag{3.7}$$

For the fourth operation region, which combines two topologies, the *0.75Vin* topology will be analyzed since it gives more SSL losses, due to the 1*Vin* topology not including any

switching. The *0.75Vin* SCVR topology is a four-phase topology, requiring four components of the SSL constant.

They are calculated in Equations (3.8), (3.9), (3.10), (3.11), and (3.12) to obtain a final result for the SSL impedance.

$$\boldsymbol{a_1 = [0, 0, 0.25, -0.25]} \tag{3.8}$$

$$\boldsymbol{a_2 = [0.25, 0.5, -0.25, -0.5]} \tag{3.9}$$

$$\boldsymbol{a_3 = [0, 0, 0.25, -0.25]} \tag{3.10}$$

$$\boldsymbol{a_4 = [0.75, -0.5, -0.25, 0]} \tag{3.11}$$

$$\boldsymbol{R_{SSL} = \frac{(0.5)^2}{C_1 f_{sw}} + \frac{(0.25)^2}{C_2 (2 f_{sw})} = \frac{0.28125}{C f_{sw}} = 0.175\ \Omega} \tag{3.12}$$

The FSL impedance, however, is entirely dependent on the switch on-resistance. The topologies are optimized so that the path of the charge from the input to the output does not contain more than three switches at any point. Accordingly, the total ESR is reduced, and the switches are selected to provide considerably lower resistance than that of the SSL resistance, which dominates the losses. Also, for the hybrid converter, the ESR of the inductor exceeds that of most other components, making the switch resistance negligible in comparison.

3.4.2 Switching Losses Minimization

The switching losses are generally a concern at lower current loads, where they would normally dominate the losses and decrease the efficiency by significant amounts. These losses are generally affected by components such as the switching frequency, the switch gate capacitances, and switching voltage, as shown in Equation (3.13).

$$\boldsymbol{P = C.V^2.f} \tag{3.13}$$

Yet, there is a more complex perspective including the effects of frequency on gate capacitance, and other components.

Switching frequency affects switching power and root mean square (RMS) resistive loss (I^2R) due to ripple current [18]. By increasing the Duty Cycle, the converter efficiency is increased due to the fact that more power is delivered to the load. If switching losses (including both the switches and the control block) are considered, they dominate the power loss in small duty cycles, reducing efficiency to 20% at a duty cycle of 10%. As a result, it can be implied that the optimum current point lies at the balance of controller-switching and resistive losses.

3.5 Simulations

For confirming proper functionality of the hybrid converter, the circuit was simulated on Multisim 14: Education Edition. Afterwards, several prototypes were implemented, utilizing different components and layouts. The PCB layout and design were based on several simulation sweeps and by using the analysis equations, for selection of the switches and modeling them.

All PCB and component parasitics were modeled and accounted for in the simulations, in order to obtain accurate figures for the expected efficiency, as well as to find the optimum operation point. The modeled parasitics include the flying capacitors ESR, inductor ESR, switches ESR, interconnects ESR, switch input capacitance, and delay resulting from switch drivers, as shown in Figure 3.2.

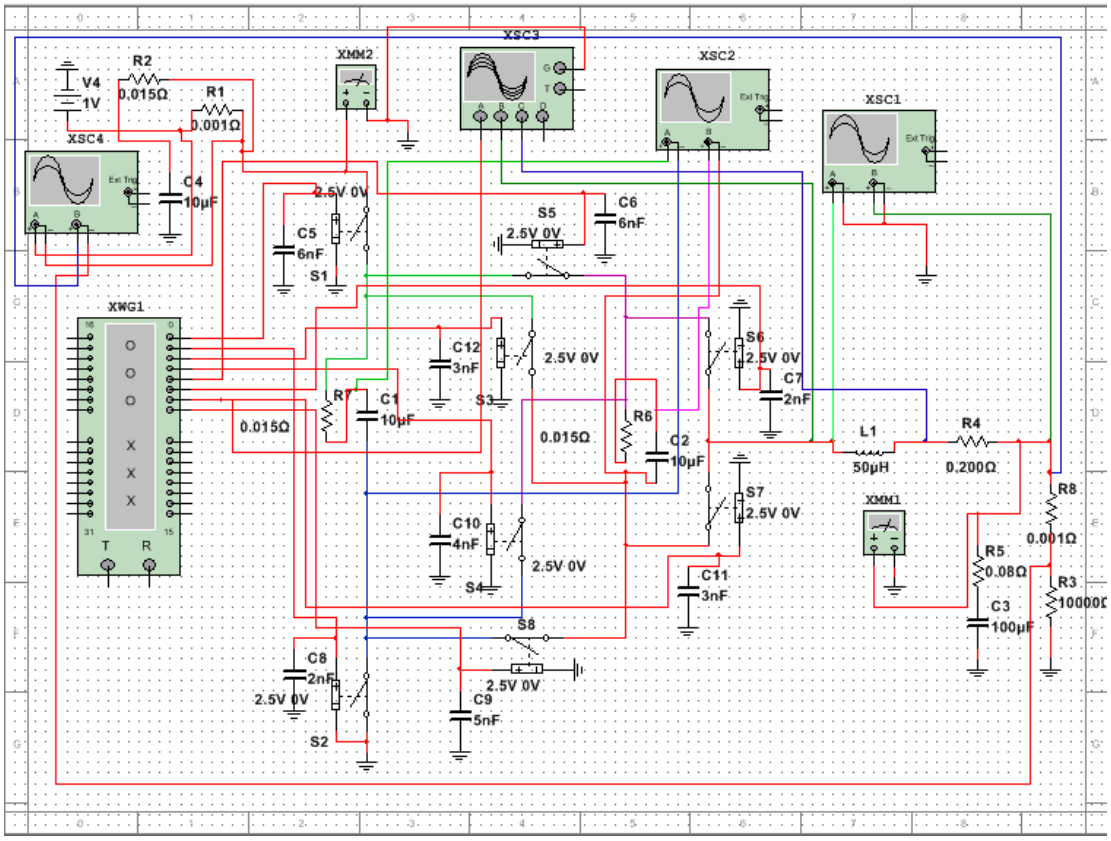

Figure 3.2. Multisim 14 circuit schematic including all parasitics and simulation tools.

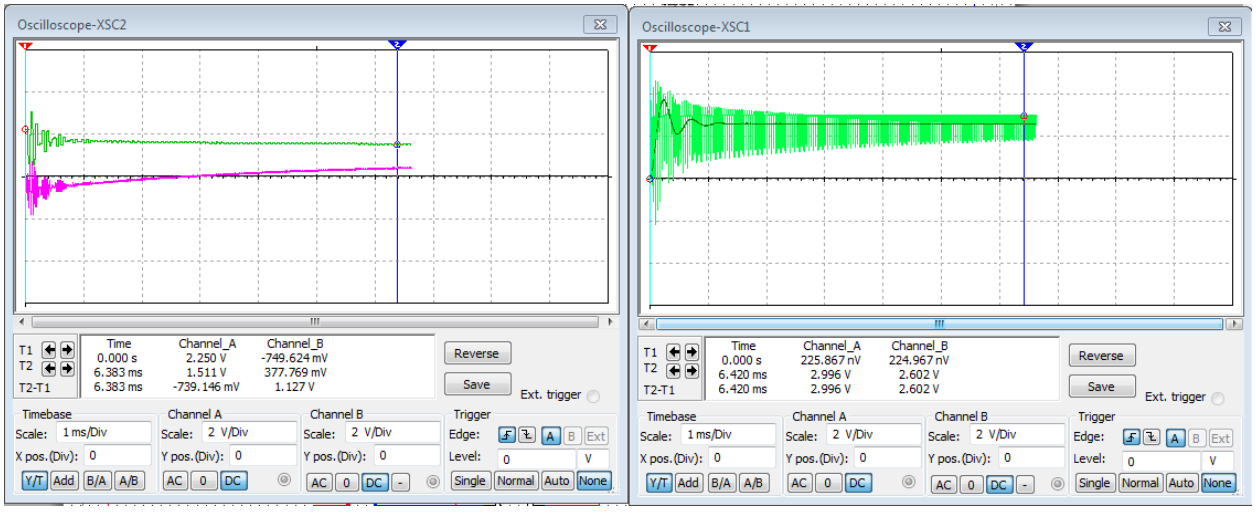

Figure 3.3. Simulated transient voltage on flying capacitors (left) and transient output voltage vs. voltage at the inductor (right)

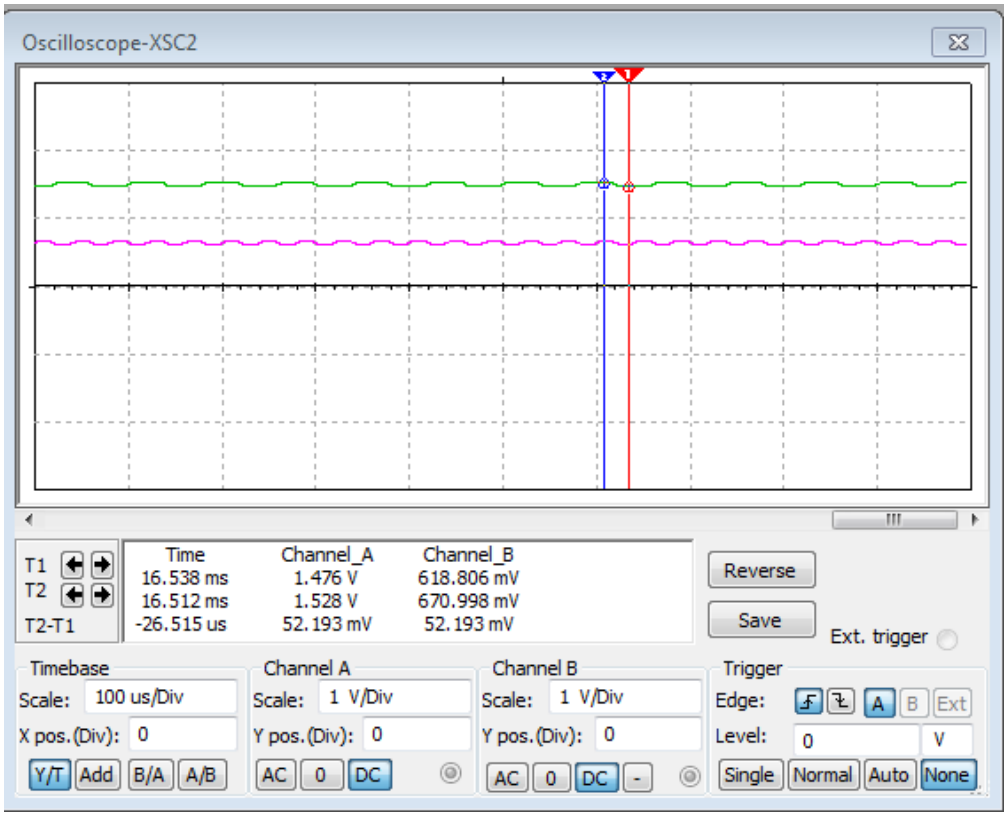

Figure 3.4. Simulated steady-state voltage on flying capacitors with C1 voltage = 0.5*Vin* and C2 voltage = 0.25*Vin* at *Vin* = 3V.

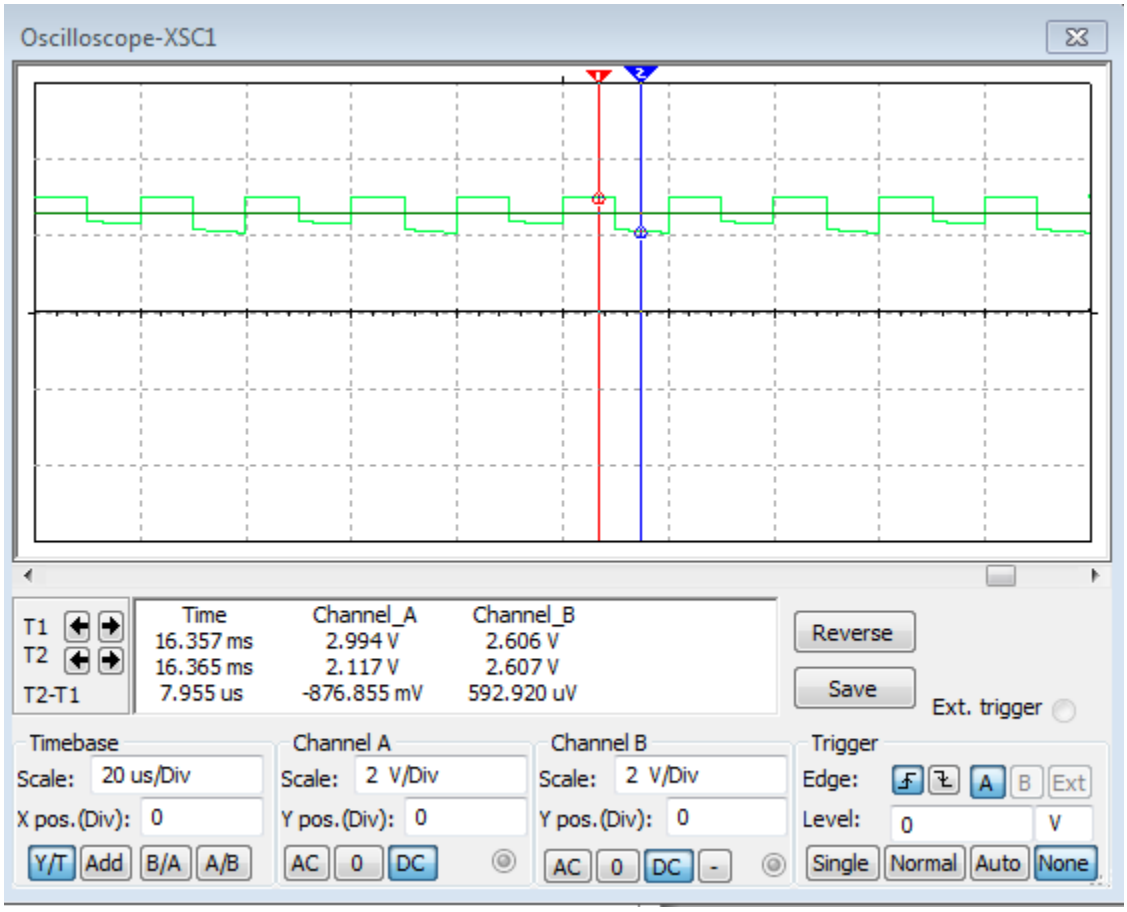

Figure 3.5. Output voltage vs. voltage at the inductor (*Vx*) in the *0.75-1Vin* operation region with *Vin* = 3V.

3.6 Control Mechanism

In order to implement the most efficient and fastest control mechanism, the control technique was adapted from the topology, as mentioned in section 3.2.2. The control technique provides high efficiency over a large bandwidth as well as simplicity in order to have a relatively small controller. Accordingly, the topology control has been implemented in order to satisfy the hybrid converter's initial design. This functions as a coarse output voltage tuning mechanism. Also, there is duty cycle control in order to obtain high efficiency while changing the output voltage and conversion ratio. Duty cycle modulation functions as a fine output voltage tuning mechanism.

Duty cycle of the even phases is changed together, while duty cycle of the odd phases is changed together. These two modulation techniques could also be expanded on to include frequency modulation without the addition of extra hardware, since the control is done by changing the code that is run on a microcontroller. Frequency would be useful to achieve better regulation at high load currents, at the expense of more losses and decreased efficiency.

The control is done by using an ATMega microcontroller by utilizing one of the 8-bit digital output ports, which controls the eight switches in the topology. The microcontroller is interfaced with the switches using MOSFET drivers, which require their own supply voltage, and their switching losses are accounted for in efficiency calculations.

3.6.1 Deadtime Implementation in the Control Signal

One of the very important aspects of the control signal was the potential overlap between two signals, causing a short circuit between the supply and the ground, which is normally avoided in buck converters by applying a deadtime between overlapping signals [22]. This has been implemented in the control signal of the hybrid converter to avoid current spikes which are caused by overlapping signals resulting from either microcontroller or driver variable delays.

3.7 Component Selection

While selecting the components, two things are taken into consideration: the values of the components and the component types. The values are determined by extensive simulations and experimentation, as well as analytical optimizations. Components include several items that are explained in the following sections.

3.7.1 Switches

Several switch types are considered when designing a high power hybrid converter. The two main types that are considered for this application are PMOS or NMOS switches. Charge transfer switches for on-chip applications are also realized using PMOS or NMOS switches, or any combination of them [4].

However, using one switch type proves to be the optimal method in order to avoid complicated driving signals, as well as mixed timing. PMOS switches generally have a different

gate capacitance than NMOS switches, which could lead to two switches overlapping if the timing signals are not adjusted properly, and this discrepancy motivates the use of a single switch type.

Accordingly, NMOS switches have been used for simplicity and due to the availability of different switches in the market. Also, NMOS switch drivers are more readily available, which allows a wider variety for selection of the optimal components.

When selecting the NMOS switches, the criteria to be met was to provide proper timing (small delay), minimal gate capacitance, minimal on-resistance, and high voltage and current ratings. Switch parasitics such as gate capacitance also increase with area and switching frequency [14]. Using a large switch would allow a small on-resistance, while using a small switch would allow smaller gate capacitance (therefore, smaller switching losses). Hence, an optimization is necessary between both factors, in order to maximize the efficiency under the same conditions, voltages, and switching frequency [12].

In the early PCB design stages, IRF 530 and IRF 510 MOSFETs were used as switches, as they provided high voltage ratings and were readily available, but had a high parasitic on-resistance and high gate capacitance. Afterwards, more appropriate, surface-mount switches were obtained and used. The primary switch of use in the final PCB has a minimal on-resistance of 5mΩ, gate capacitance of 2000pF, and maximum ratings of about 20V between the drain and source.

3.7.2 Capacitors

The use of ceramic capacitors for the flying capacitors is necessary to reduce the parasitic resistances. It is known that to get higher efficiency, capacitors with lower ESR and MOSFETS with lower on-resistance are preferred [10]. Therefore, ceramic capacitors are found to be the capacitors with least ESR, but the capacitance values that could be reached are limited, and for surface-mount capacitors it is even more limited. Increasing the flying capacitor size is important for charge transfer, and becomes a determining factor for the maximum load current, along with the frequency of operation [14] [17].

Also, maximum capacitor ratings are important since they determine the maximum voltage and temperature possible for operation. Therefore, the highest ratings are selected in order to provide maximum durability under stressful conditions on high power. Accordingly, X7R capacitors are used, which provide the highest temperature ratings possible. Also, the voltage rating is up to 16V, which gives a wide voltage range since the capacitors are not charged to more than half of the input voltage.

For selection of the capacitance, a method was used that is proposed by Seeman which provides the optimal capacitance for a given topology, yielding the maximum efficiency [19]. Yet, another technique is adapted from [30] to further optimize capacitance value. A sweep of different capacitance values was implemented for the *0.75Vin* topology, and the maximum was achieved at a range between 5-10uF.

As for the output capacitor, it was selected to be a tantalum capacitor in order to achieve accuracy and a high value for the capacitance. The accuracy of tantalum capacitors is generally known to be much higher than that of electrolytic capacitors, and is therefore preferred. A strategy to limit the peak current is by decreasing the ESR and increasing the output capacitance. High frequency and large capacitor RC can also reduce peak current.

Therefore the capacitor selected should be a surface mount capacitor with high value (around 100uF) to have the least noise and voltage ripple possible. The value is also optimized for the LC time constant of the inductive filter to be larger than the switching period, in order to have the right functionality mentioned in [24] and [27].

3.7.3 MOSFET Drivers

For the MOSFET drivers, the main criteria were delay and power consumption. First, High-Side MOSFET drivers are considered since they will allow smaller driving voltages and would reduce the switching power losses. However, one type was implemented in the early PCBs, with very mixed outputs. That was primarily due to the imperfect connections between the nodes, and the wiring complexity of peripheral components (such as diodes and capacitors) around the MOSFET drivers. Therefore, a simpler alternative was selected, which is using Low-

Side MOSFET drivers which operate at a wider range of output voltages, with no overhead components.

3.7.4 Inductance

The inductance is an optimization between the components in Equation (3.5), where increasing the inductor size allows decreased ripples or decreased frequency of operation at the same output ripples. Yet, there are restrictions on the maximum inductance value, since large inductors take up a lot of area and are difficult to place in compact designs.

Increasing the switching frequency of the converter or using multiphase technology such as the one used in the hybrid converter can reduce the size and weight of the inductor, but it also increases the switching power loss and produces difficulties for thermal management. Therefore, the 5-Level Hybrid converter provides an alternative, which is decreasing the output voltage ripples by four times in order to reduce the inductor size accordingly.

A coil-wound inductor was selected with minimal ESR in order to minimize the conduction losses. However, the advantage of the 5-Level Hybrid converter over a standard buck converter is mainly apparent when the application limits the inductor size. Accordingly, a relatively small inductor size for the application is used in order to simulate conditions when there are strict limitations on inductor size. Also, the inductor quality factor is kept low since these are the conditions where the hybrid converter excels, and when the performance of the buck converter is not optimal.

3.8 Optimization and Layout Considerations

Optimizing the converter efficiency could be further done by improving switch conductance and gate capacitance, improving capacitor technology (for a higher capacitor density), reduction of charge transfer switches parasitics, and adding a control mechanism for power backoff at low load currents.

When designing the PCB layout, some aspects were considered in order to obtain the best possible performance. First, the primary tracks connecting the path from the input voltage to the capacitors, and from the capacitors to the output, through the switches, were analyzed and

prioritized in terms of decreasing their length and increasing their width. Then, proper grounding is ensured to achieve proper functionality from the MOSFET drivers without any ripples.

3.9 PCB Implementations

For the implementations, five prototypes were used, utilizing different components and layouts. The PCB layout and design were based on several simulation sweeps and by using the analysis equations, for the selection and modeling of the switches. The process of implementing five different PCB prototypes is described in the following sections, with an analysis of each PCB's results and the conclusions obtained.

3.9.1 First PCB

3.9.1.1 First PCB Components

The initial design was implemented on a breadboard using the components in Table 3.3. Next, it was moved to a PCB for better testing and performance. The components were obtained based on local market availability and the values were optimized based on several simulations and calculations. This was done to achieve the highest possible performance.

Table 3.3. Components used for Printed Circuit Board #1.

Component	**Component Type and Details**
Flying Capacitors	Electrolytic Capacitors 22uF
Switches 1-8	IRF 510 NMOS
Inductor	Air-Core Inductor 2.2uH
Output Capacitor	Electrolytic Capacitor 120uF
Frequency	1 MHz

The IRF510 NMOS transistors were selected since they had acceptable specifications including an average threshold voltage, average on-resistance, and high voltage ratings. The

electrolytic flying and output capacitors were used because ceramic capacitors (which have decreased losses) are not locally available in large capacitances (higher than 1uF). The air core inductor was used because it provided an acceptable quality factor with low series impedance, since it is a coil-wound inductor.

3.9.1.2 First PCB Results

The result of the selected components was correct functionality with very low efficiency that was below 20% conversion efficiency. However, the main limitation was the parasitic resistances in the components. For starters, the switch on-resistance is about 500mΩ per switch, and there are three switches in the path from the input voltage to the output voltage. When compared to a 10Ω load, the switch parasitic resistances consume 15% of the input power. Also, the electrolytic switching and output capacitors have a high ESR, which would result in increased losses. Finally, the lack of an interface between the microcontroller and the switches resulted in inaccurate driving signals, which further decreased the efficiency.

3.9.1.3 First PCB Conclusion

In order to achieve higher efficiency and better overall performance, it is necessary to use more appropriate switches that are designed for this particular application, as well as ones with decreased on-resistance for improved performance. Moreover, ceramic capacitors needed to be used to obtain smaller parasitic resistance for high switching frequency. Minimization of the switching frequency is also expected to lead to decreased switching losses, which would increase the overall efficiency. The addition of an interface stage between the controller and the switches is also necessary in order to increase the driving voltage, which would further decrease the switch on-resistance. Finally, an inductor with a high quality factor is also recommended for future implementations since it would further boost the efficiency.

3.9.2 Second PCB

3.9.2.1 Second PCB Components

The second PCB prototype, built with the components from Table 3.4, proved to be more promising. The results were expected to be higher than in the first PCB.

Table 3.4. Components used for Printed Circuit Board #2.

Component	Component Type and Details
Flying Capacitors	X7R Ceramic Capacitors 10uF
Switches 1-8	SI3460 NMOS
Inductor	Coil-Wound Inductor 2.2uH
Output Capacitor	Tantalum Capacitor 100uF
MOSFET Drivers	LTC4440
Frequency	125 kHz

First, the components were selected based on their ESR and power ratings. The NMOS transistors each had an on-resistance of 25mΩ, which reduces the path resistance from 1.5Ω in PCB 1 to about 75mΩ in PCB 2.

Secondly, the addition of a MOSFET driver before every switch as an interfacing stage provided more accurate signals and better driving. This leads to the switches turning on fully, which maximizes the efficiency. However, the MOSFET drivers that were used required peripheral diodes and ceramic capacitors, which were added in a separate PCB. Accordingly, the interface board containing the drivers, shown in Figure 3.6, was mounted below the converter PCB, which contains the switches and other components.

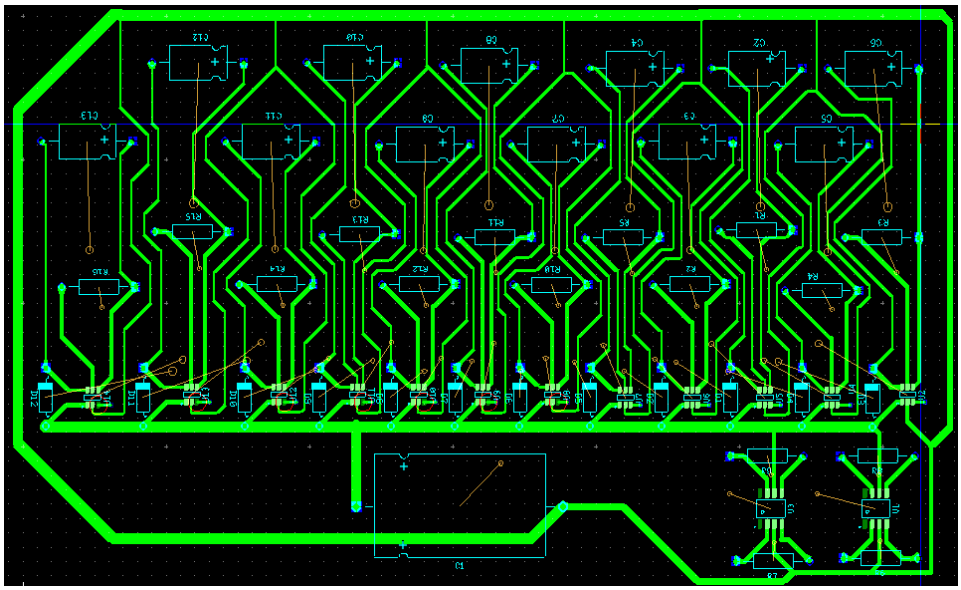

Figure 3.6. First MOSFET drivers Printed Circuit Board.

Third, ceramic capacitors, more appropriate for switching due to their low ESR, were used instead of with tantalum capacitors. The ceramic capacitor used is shown to have a low ESR at a multitude of frequencies in Figure 3.7; it is clear that at any frequency of use, a maximum ESR of 15mΩ could be found, which is negligible when compared to the much higher load resistance. The addition of ceramic X7R capacitors instead of X5R proved to be the optimal choice due to their increased reliability at high load currents as well. A tantalum capacitor superior to an electrolytic capacitor, in terms of tolerance, is used for the output capacitor. Tantalum capacitors are also able to achieve high values, which are out of the ceramic capacitors' range.

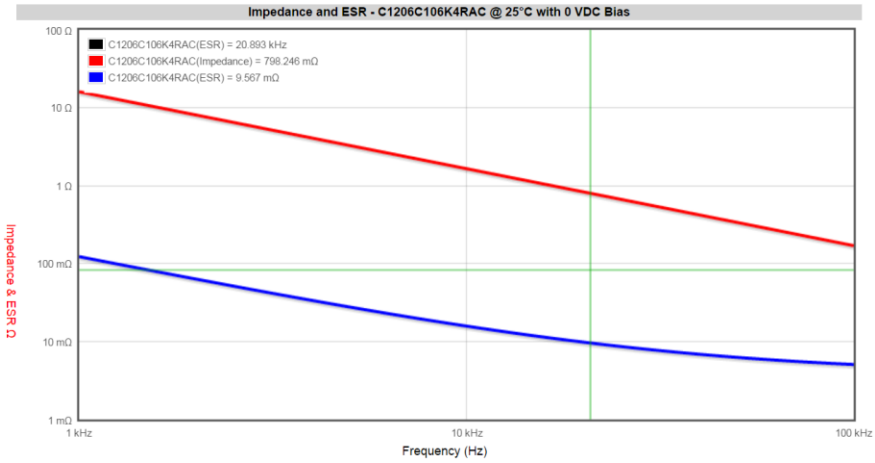

Figure 3.7. Flying Capacitor ESR (mΩ) vs. Frequency (Hz).

3.9.2.2 Second PCB Results

However, the layout, shown in Figure 3.8, was imperfect, leading to several limitations, such as the high parasitic track resistance, which significantly reduced the efficiency as well. This also led to correct functionality, but the efficiency suffered and reached a maximum of 30% conversion efficiency excluding switching losses. Accordingly, several improvements were necessary to optimize the design to achieve higher performance.

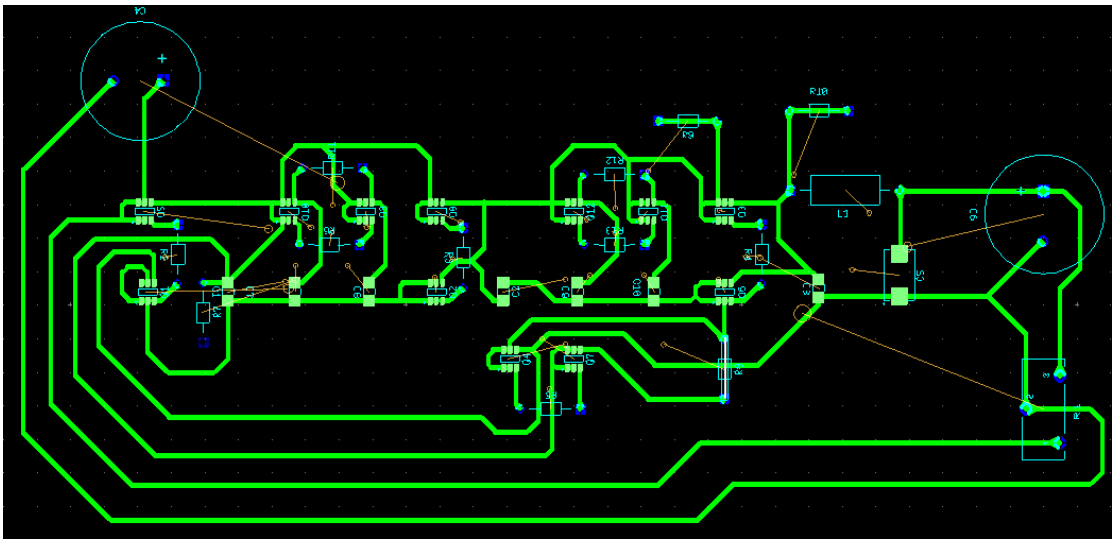

Figure 3.8. Printed Circuit Board #2 Layout.

3.9.2.3 Second PCB Conclusion

It is evident that the second PCB had major flaws that needed to be addressed in order to further improve the performance. First, a more optimized layout would achieve higher efficiency, since long tracks result in relatively high parasitic impedance which dominates the conduction losses. Also, improving the switches is necessary since they were frequently damaged by testing the circuit, on account of to their low voltage rating. The necessity of these modifications became apparent after extensive measurements and trials, and they were found to be the only possible course of action.

3.9.3 Third PCB

3.9.3.1 Third PCB Components

For the third PCB, a new switch type was used, which provided lower ESR, higher voltage rating, and smaller footprint, since two NMOS transistors were found in each IC. The components used are found in Table 3.5 for reference. The layout of the components was also optimized in order to decrease the parasitics.

Table 3.5. Components used in Printed Circuit Board #3.

Component	Component Type and Details
Flying Capacitors	X7R Ceramic Capacitors 10uF
Switches 1-8	SI7236DP NMOS
Inductor	Shielded Coil-Wound Inductor 2.2uH
Output Capacitor	Tantalum Capacitor 100uF
MOSFET Drivers	LTC4440
Frequency	125 kHz

3.9.3.2 Third PCB Results

The PCB layout, shown in Figure 3.9, was imperfect due to relatively long traces, as well as high parasitics caused by the imperfect process. Nevertheless, correct functionality at a low efficiency of 30% was obtained. The circuit was also much more reliable due to the use of higher voltage rated switches. This proved to be a valuable lesson where components rated voltages became necessary to always be considered with a safety factor, since using voltages that are close to the maximum ratings results in component damage.

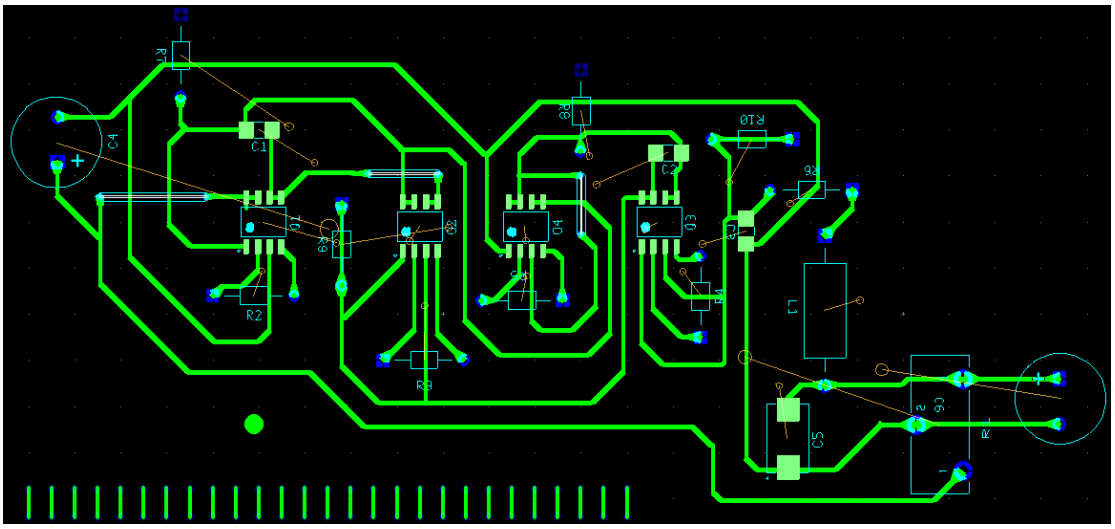

Figure 3.9. Printed Circuit Board #3 Layout.

3.9.3.3 Third PCB Conclusion

These results needed further improvements in terms of components selection, and more importantly, layout optimization. First, the MOSFET drivers' signals were measured and found to be inaccurate. Second, the drivers required multiple peripheral components which increased the overall area and the switching power losses. Hence, a new MOSFET driver type was necessary for increased efficiency and more accurate functionality. Furthermore, the switches needed further improvement in terms of layout in that they needed to be closer to have smaller, thicker tracks connecting them. Finally, the switching losses were very high, and needed more optimization by decreasing the switching frequency. These minor modifications promised higher performance and even decreased total area, in order to achieve a compact, efficient PCB.

3.9.4 Fourth PCB

3.9.4.1 Fourth PCB Components

In the fourth attempt, different MOSFET drivers with smaller footprint and no peripheral requirements were used. These were easily integrable on the main converter PCB, along with the other components. However, due to switching power losses, the operating frequency was reduced to optimize total efficiency. This was compensated by increasing the inductor size slightly to obtain maximized performance at the current operating conditions. The components used in the fourth PCB are found in Table 3.6.

It is clear that the layout, found in Figure 3.10, is optimized for minimal parasitic resistance. Thicker tracks and shorter paths were constructed between the input and output in order to maximize the efficiency. Figure 3.11 shows the PCB before mounting the components, and Figure 3.12 shows the final PCB, with a US quarter dollar for scale.

Table 3.6. Components used in Printed Circuit Board #4.

Component	**Component Type and Details**
Flying Capacitors	X7R Ceramic Capacitors 10uF
Switches 1-8	SI7236DP NMOS
Inductor	Coil-Wound Inductor 50uH
Output Capacitor	Tantalum Capacitor 100uF
MOSFET Drivers	LM5111
Frequency	20 kHz

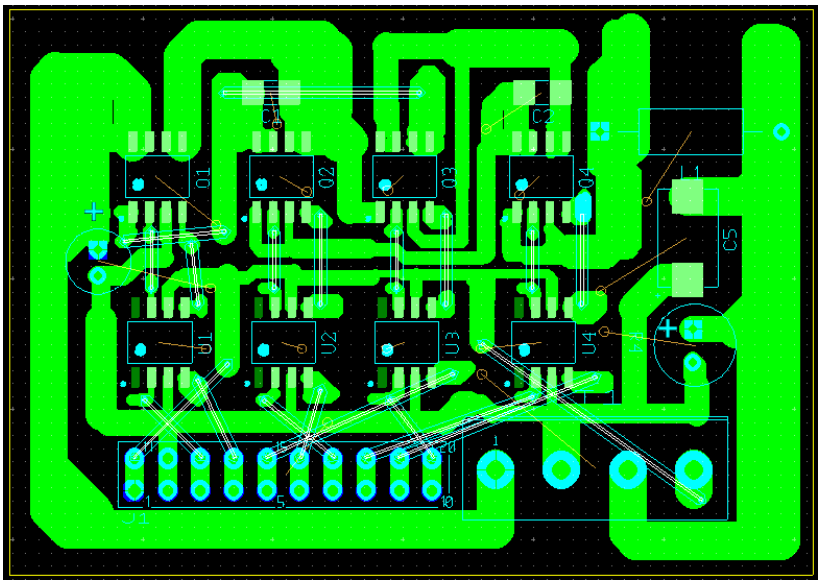

Figure 3.10. Printed Circuit Board #4 Layout.

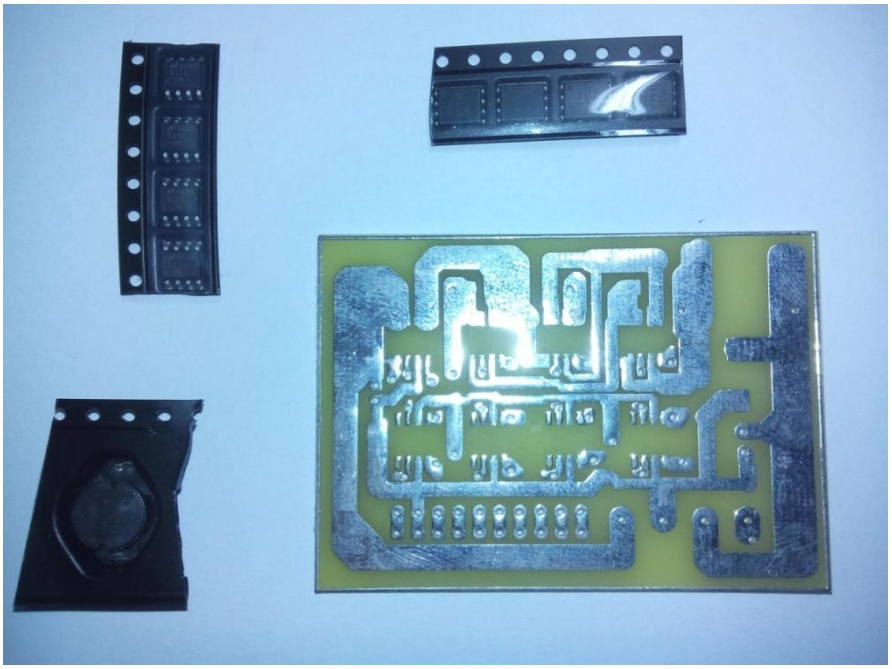

Figure 3.11. Printed Circuit Board #4 before components mounting.

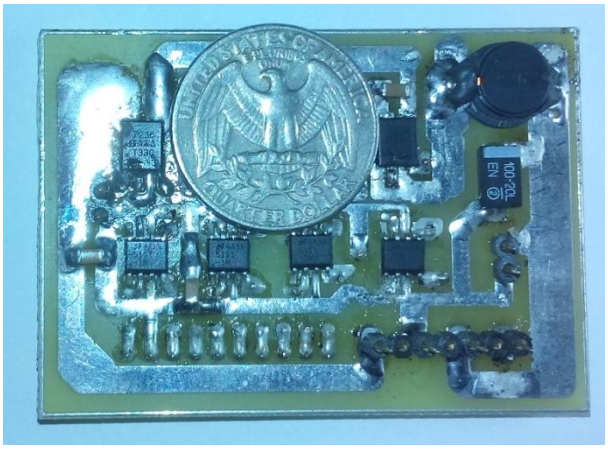

Figure 3.12. Completed Printed Circuit Board #4 with US quarter dollar for scale.

3.9.4.2 Fourth PCB Results

The new compact PCB achieved high efficiency, in the range of 90%, including all switching and conduction losses. These results were obtained due to perfect functionality and balance of the capacitor voltages on the correct levels. This decreased the parasitic losses caused by charging and discharging the capacitors too often. Also, the new MOSFET drivers proved to achieve accurate driving signals, while consuming relatively small dynamic power, and virtually no static power. This allowed a reduction of the switching losses, especially at high power conversion.

3.9.4.3 Fourth PCB Conclusion

At small loads, the losses were mainly dominated by the switching losses, which needed further optimization. This is proposed to be solved by decreasing the switch gate capacitance, which is directly proportional to switching power losses. This necessitates the use of more efficient NMOS power transistors with smaller gate capacitance, while maintaining or improving the on-resistance. Another improvement is making the traces even thicker, to sacrifice some of the area for higher efficiency, since the layout proved to be very compact despite the large number of components.

3.9.5 Fifth PCB

3.9.5.1 Fifth PCB Components

Finally, the last PCB was implemented by using different switches, which had a slightly larger footprint, but with much higher performance. The new switches, found in the Table 3.7, provided lower ESR, and lower gate capacitance. This allowed a reduction of both conduction and switching losses. However, the cost was a lower voltage and current rating, which is shown in a comparison between the different types of switches used throughout the process in Table 3.8.

The final layout, shown in Figure 3.13, was also compact in order to decrease any conduction losses caused by parasitic resistances. The traces can be seen to be thick and short for maximum efficiency, as is shown in Figure 3.14 with the PCB before mounting the components. Finally, the PCB with all components mounted is found in Figure 3.15, with a US quarter dollar for scale.

Table 3.7. Components used for Printed Circuit Board #5.

Component	**Component Type and Details**
Flying Capacitors	X7R Ceramic Capacitors 10uF
Switches 1-8	STL100N1VH5 NMOS
Inductor	Coil-Wound Inductor 50uH
Output Capacitor	Tantalum Capacitor 100uF
MOSFET Drivers	LM5111
Frequency	20 kHz

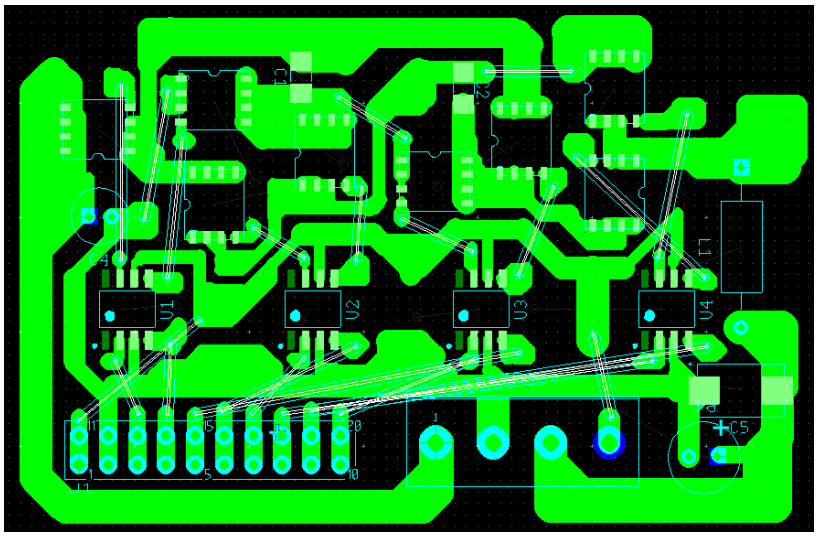

Figure 3.13. Printed Circuit Board #5 layout.

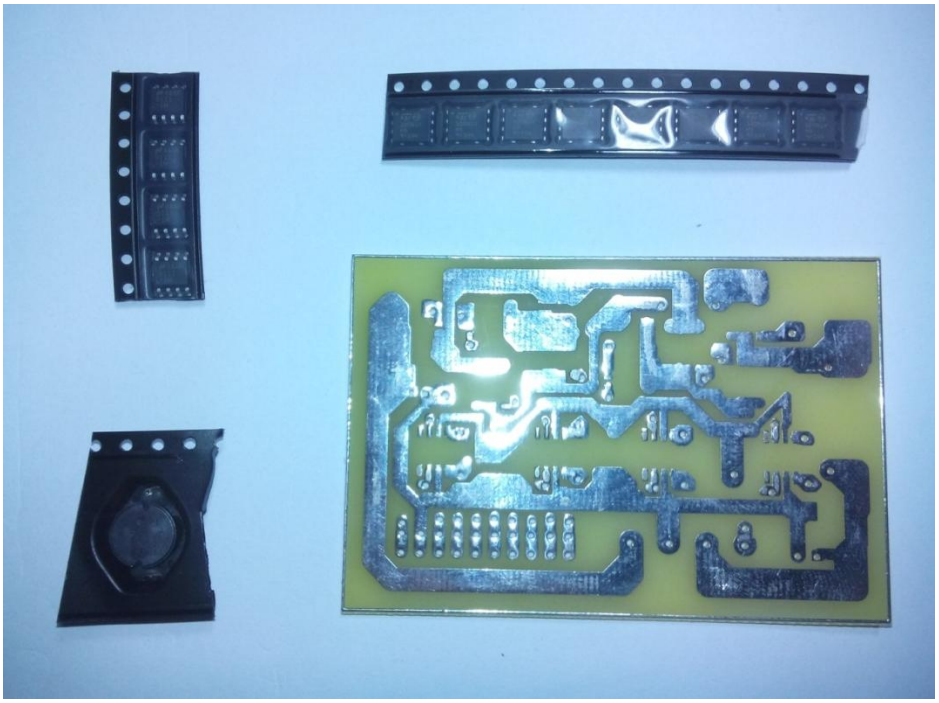

Figure 3.14. Printed Circuit Board #5 before components installation.

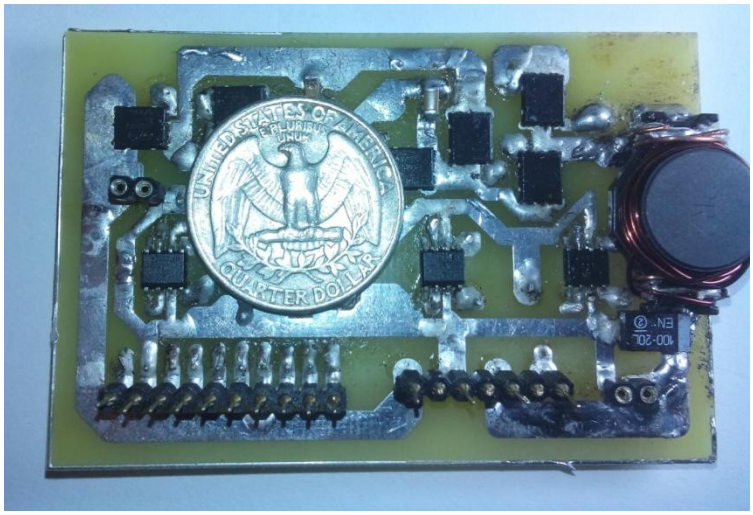

Figure 3.15. Completed Printed Circuit Board #5 with US quarter dollar for scale.

3.9.5.2 Fifth PCB Results

High efficiency was obtained with the fifth and final PCB as a result of switching losses reduction as well as conduction loss reduction. Peak efficiency of up to 94% is achieved with the final PCB, with the complete results and analysis exhibited in Chapter 5. High efficiency was obtained for a wide range of conversion ratios, all the while including all sources of power loss. The test setup and the testing workstation are also shown in Figures 3.16 and 3.17.

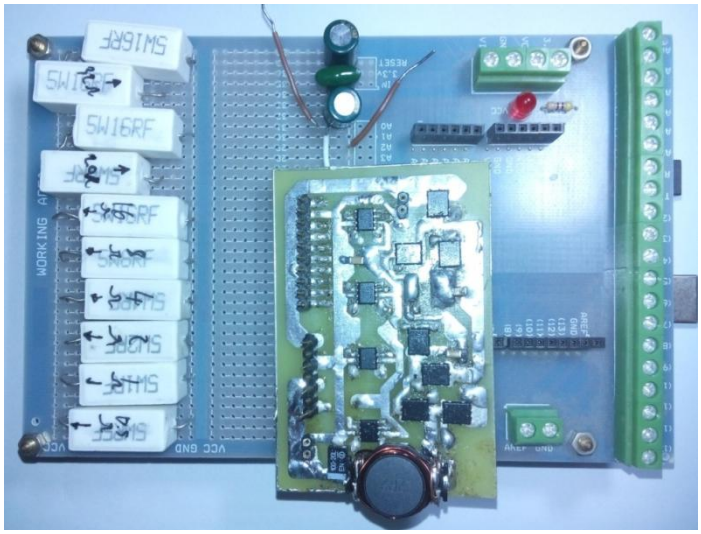

Figure 3.16. Test setup with the converter Printed Circuit Board #5, microcontroller, peripheral decoupling capacitors, and load resistances.

Figure 3.17. Workstation used for testing.

3.9.5.3 Fifth PCB Conclusion

Optimizing the components proved to be a challenging but crucial task, which achieved high performance by the 5-level hybrid topology. This was done by minimizing the components ESR, and ensuring proper functionality. The MOSFET switches were optimized through a long process with several considerations during the selection. Between the first and last PCB implementation, four types of NMOS transistors were used, which are shown and compared in Table 3.8. It is clear that towards the fifth implementation, the on-resistance was minimized to achieve the minimum possible parasitic losses, and the gate threshold voltage was decreased to ensure proper functionality while maintaining high component power ratings for increased reliability.

Table 3.8. Comparison between different Metal-Oxide Silicon Field-Effect Transistor switches used in all Printed Circuit Boards.

Type of MOSFET	**On-Resistance**	**Gate Capacitance**	**Maximum Drain-Source Current**	**Gate Threshold Voltage**
IRF 510 NMOS	0.540 Ω	135pF	5.6A	4V
SI3460 NMOS	0.027 Ω	1200pF	6A	0.45
SI7236DP NMOS	0.0070 Ω	4000pF	60A	1.5V
STL100N1VH5 NMOS	0.003 Ω	2000pF	25 A	0.5V

Further enhancements would be possible by more optimization of the layout, along with more integration of the components to include the controller, for a more compact converter.

3.10 Chapter Summary

The 5-level hybrid converter topology was adapted and simulated for a PCB implementation. The aim is to test the topology for proper functionality and high performance, using a high power PCB implementation. Multiple implementations of the 5-level hybrid converter were done with different components and the outputs were measured. The components were selected based on criteria for maximum efficiency and minimum footprint area.

The five PCB implementations faced several challenges, and the process was improved so that the final implementation overcame all of these challenges. In the fifth and final PCB implementation, a high efficiency of 94%, including all conduction and switching losses, was reached. The measured circuit voltage waveforms and graphs of the final implementation with optimized performance and ideal functionality are demonstrated and discussed in the following chapter.

Chapter 4

RESULTS AND DISCUSSION

4.1 5-Level Hybrid Testing and Measurements

The 5-Level Hybrid Converter was tested at input voltages of 3V and 5V, using load resistances from 1Ω to 32Ω. Peak efficiency of 94% was reached, including switching losses and conduction losses.

Correct operation and functionality was confirmed by measuring the voltage at the inductor input (*Vx*) on an oscilloscope, which proved accurate switching between the two levels being tested. The inductor input voltage is demonstrated throughout the chapter, and the voltage ripple is compared to that of buck and 3-level implementations using the same components and tested under the same conditions.

4.1.1 Voltage at the Inductor (*Vx*) Waveforms

4.1.1.1 *0-0.25Vin* Operation Region

The voltage at the inductor is shown in Figure 4.1 to be between 0 and 740mV for the *0-0.25Vin* operation region at *Vin*=3V, at a 50% duty cycle. The same is found for a 25% duty cycle, as shown in Figure 4.2.

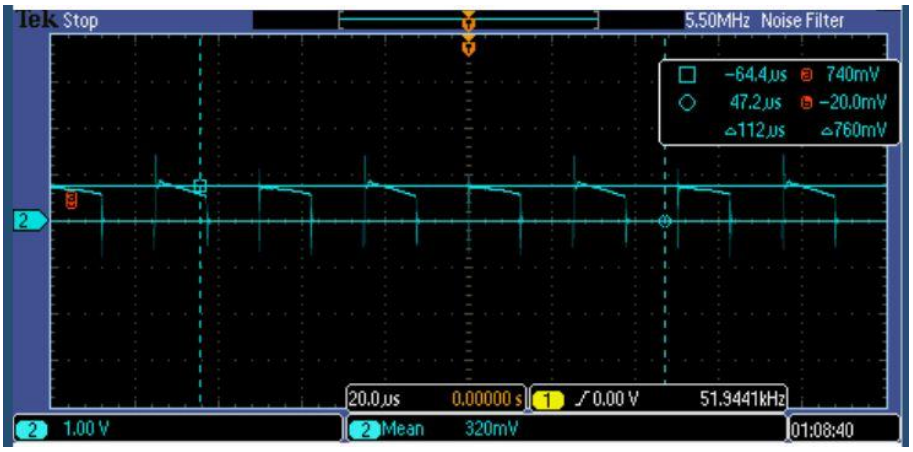

Figure 4.1. Voltage at the Inductor (*Vx*) for the *0-0.25Vin* operation region with 50% duty cycle.

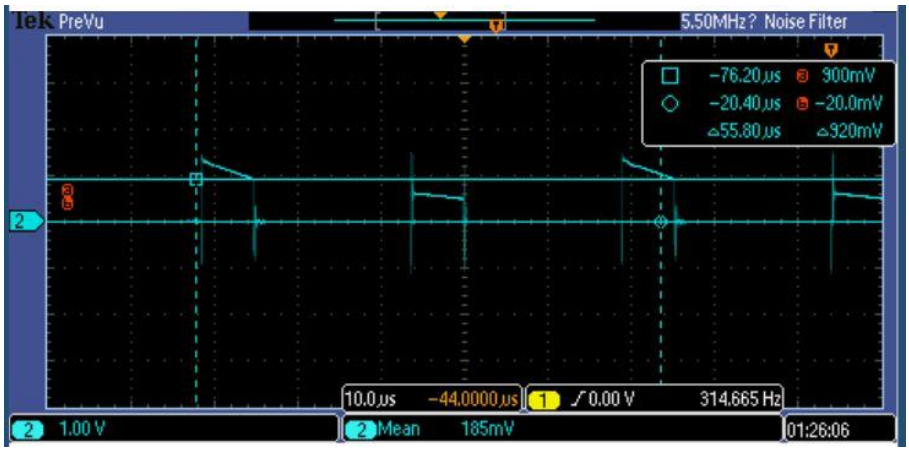

Figure 4.2. Voltage at the Inductor (*Vx*) for the *0-0.25Vin* operation region with 25% duty cycle.

As displayed by the figures above, the voltage at the inductor proves proper functionality at this operation region, and varying the duty cycle produces a direct effect on the waveform and the output voltage, which is the average voltage.

4.1.1.2 *0.25-0.5Vin* Operation Region

For the second operation region, *0.25-0.5Vin*, Figures 4.3 and 4.4 show proper operation where the two voltage levels are 780mV to 1.5V at *Vin*=3V, with 40% duty cycle.

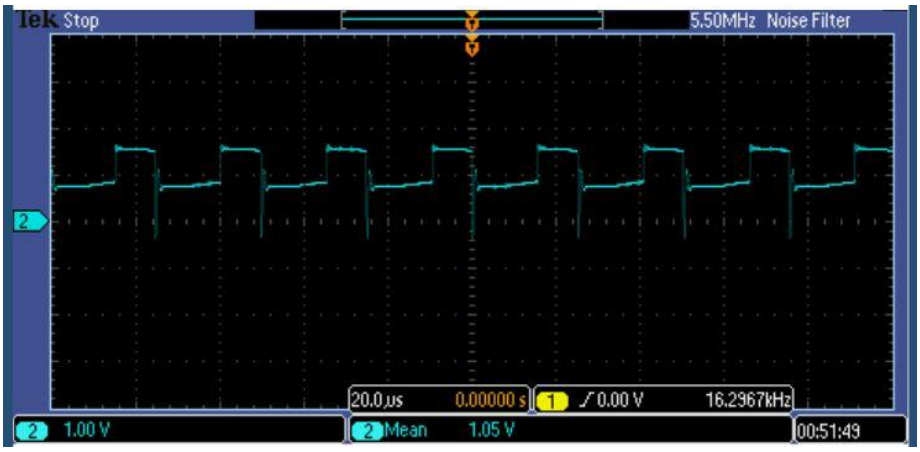

Figure 4.3. Voltage at the Inductor (*Vx*) for the *0.25-0.5Vin* operation region with 40% duty cycle.

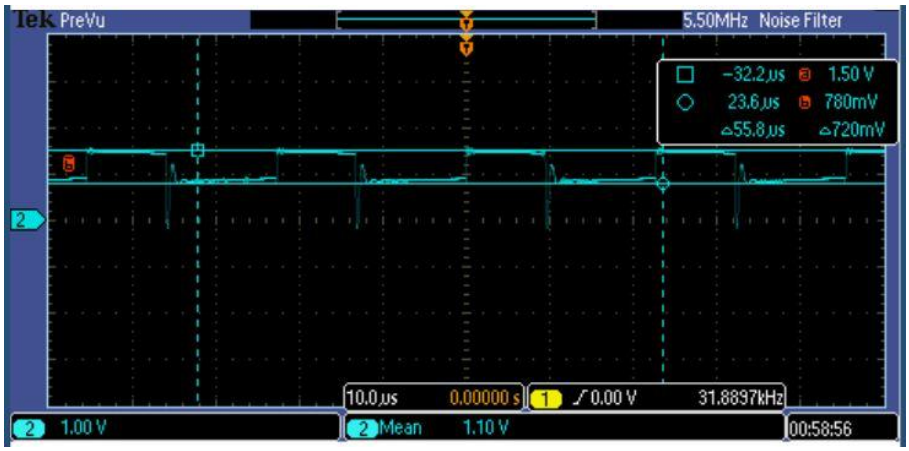

Figure 4.4. Voltage at the Inductor (*Vx*) for the *0.25-0.5Vin* operation region with 40% duty cycle with cursors.

For the *0.25-0.5Vin* operation region, the waveforms also prove correct functionality with the same voltage ripple of 0.25*Vin*, which is proven to be the maximum voltage ripple.

4.1.1.3 *0.5-0.75Vin* Operation Region

As for the *0.5-0.75Vin* operation region, Figures 4.5 and 4.6 show the two levels being 1.46V and 2.3V, with 50% duty cycles, for the same 3V input. Also, Figures 4.7 and 4.8 show the two levels at 25% and 75% duty cycles.

Figure 4.5. Voltage at the Inductor (*Vx*) for the *0.5-0.75Vin* operation region with 50% duty cycle.

Figure 4.6. Voltage at the Inductor (*Vx*) for the *0.5-0.75Vin* operation region with 50% duty cycle with cursors.

At 50% duty cycle with a 3V input, the average output voltage for the *0.5-0.75Vin* operation region is ideally between 1.5V and 2.25V, which is 1.875V. It is shown that the output is around 1.81V, due to parasitic losses. Moreover, reducing the duty cycle to 25% produces a lower output voltage of 1.64V and increasing the duty cycle results in a higher output voltage of 2.08V. This ensures that virtually any output voltage is feasible for the duty cycle modulation within the 5-level hybrid.

Figure 4.7. Voltage at the Inductor (*Vx*) for the *0.5-0.75Vin* operation region with 25% duty cycle.

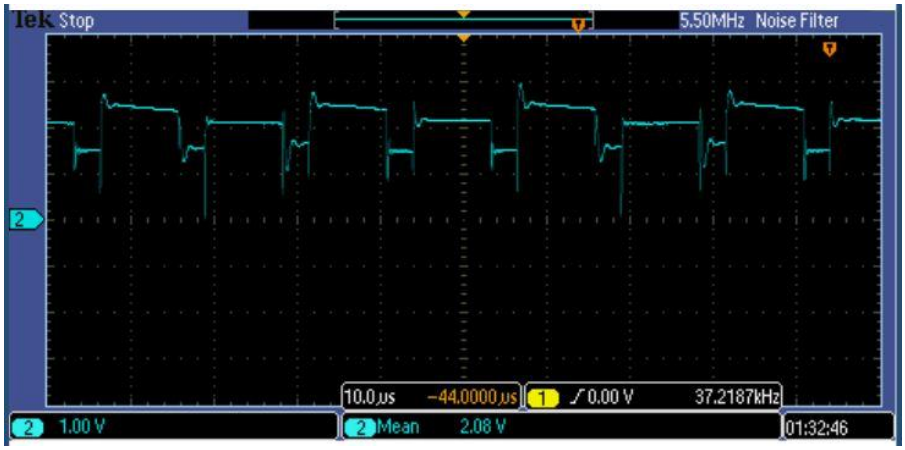

Figure 4.8. Voltage at the Inductor (*Vx*) for the *0.5-0.75Vin* operation region with 75% duty cycle.

4.1.1.4 *0.75-Vin* Operation Region

Finally, Figures 4.9, 4.10, and 4.11 show proper functionality at *0.75-1Vin* with the two levels being 2.26V to 3V, at 50% duty cycles. Figures 4.12 and 4.13 show the two levels at 25% and 75% duty cycles.

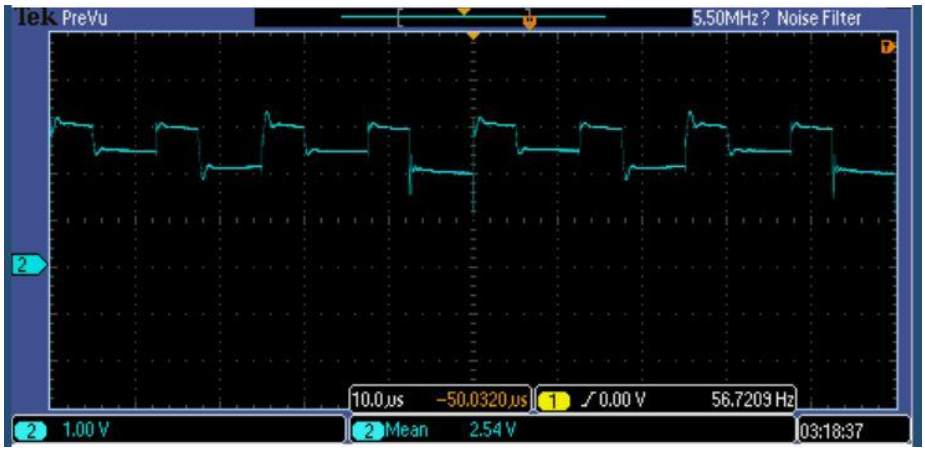

Figure 4.9. Voltage at the Inductor (*Vx*) for the *0.75-1Vin* operation region with 50% duty cycle.

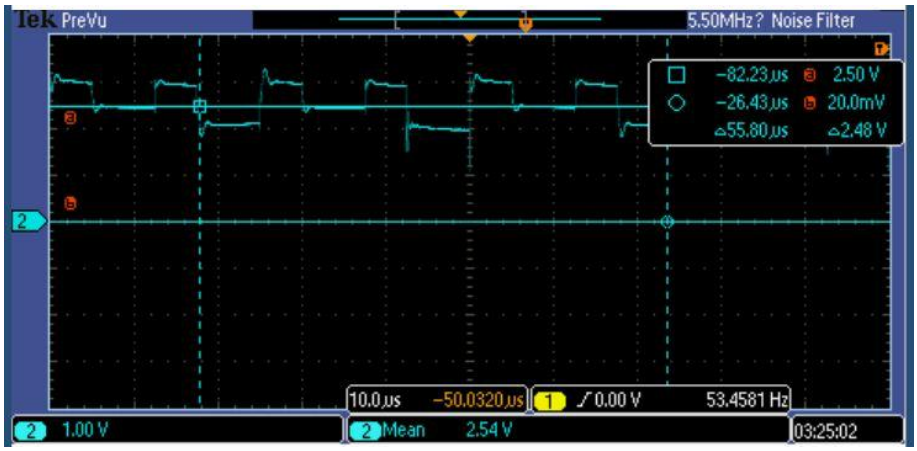

Figure 4.10. Voltage at the Inductor (*Vx*) for the *0.75-1Vin* operation region with 50% duty cycle with cursors on average.

The resulting output voltage from using 50% duty cycle in the highest operation region is 2.54V, which is very close to the ideal voltage of 2.625V. This minor difference in voltage is caused by the small parasitic impedance in the PCB traces, the switch on-resistance, and other components ESR. For regulation purposes, a higher duty cycle can be used to obtain the ideal 50% duty cycle output voltage, in order to compensate for the intrinsic parasitic losses.

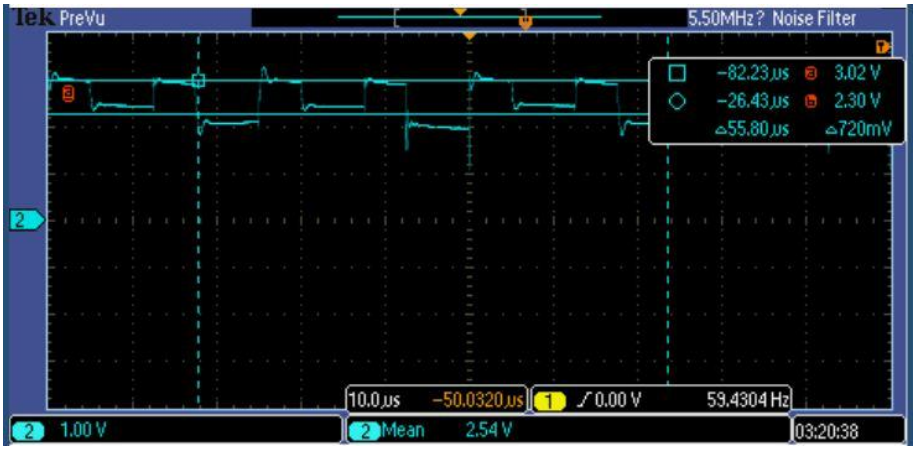

Figure 4.11. Voltage at the Inductor (*Vx*) for the *0.75-1Vin* operation region with 50% duty cycle with cursors on both output levels.

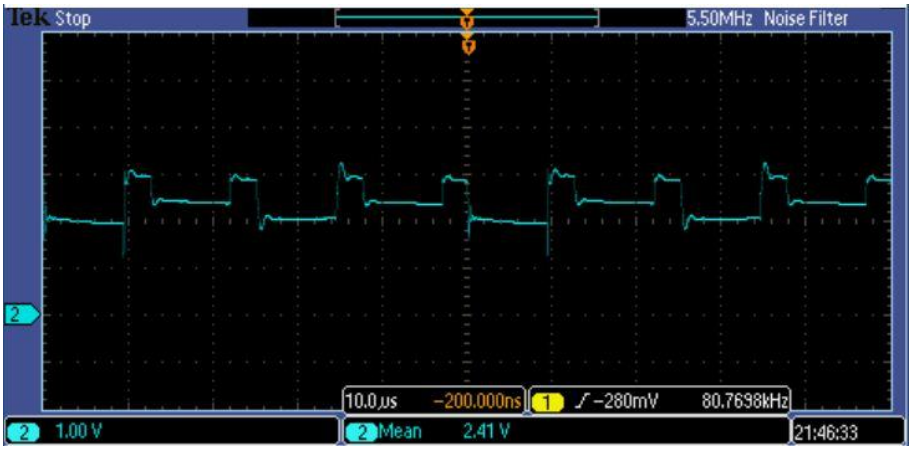

Figure 4.12. Voltage at the Inductor (*Vx*) for the *0.75-1Vin* operation region with 25% duty cycle.

Varying the duty cycle to 25% or 75% provides lower and higher output voltages of 2.41V and 2.79V, which demonstrates the wide range of conversion ratios achieved by the fine tuning duty cycle modulation. This demonstrates the versatility of the 5-level in producing different waveforms at the inductor input by utilizing the SCVR to reduce the voltage ripple.

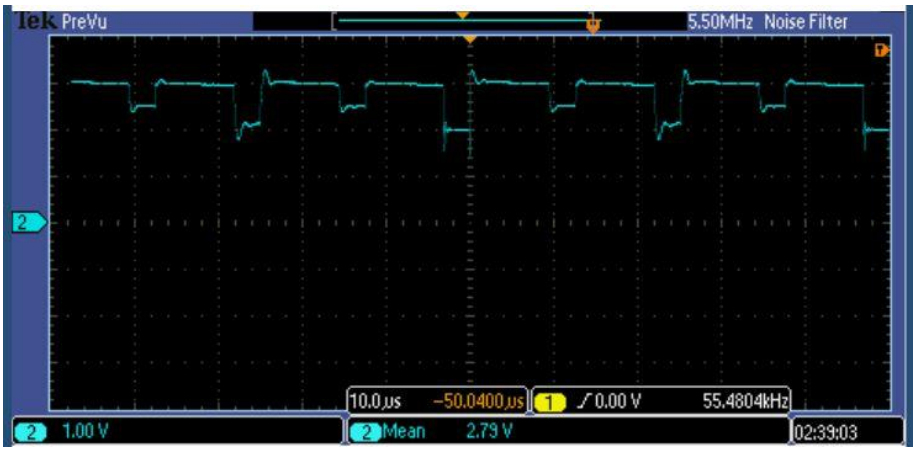

Figure 4.13. Voltage at the Inductor (*Vx*) for the *0.75-1Vin* operation region with 75% duty cycle.

4.1.2 Flying Capacitors Operation

As for the flying capacitors, the voltage on C1 is shown in Figures 4.14 and 4.15 to be between 1.5V to 1.75V at *Vin*=3V, where the optimal voltage on C1 is 0.5*Vin*. As for C2, the voltage is shown in Figure 4.16 to be between 250mV and 560mV, where the optimal voltage is 0.25*Vin*, and is reduced due to conduction losses and a high load current.

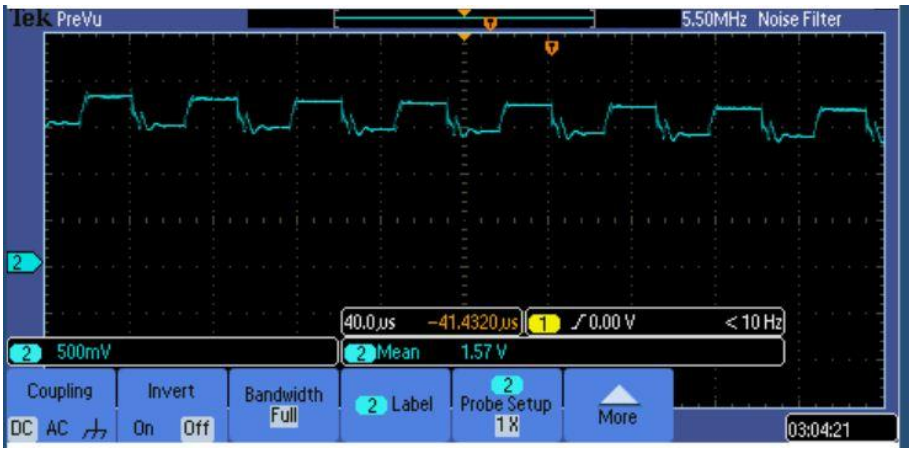

Figure 4.14. Voltage on flying capacitor C1.

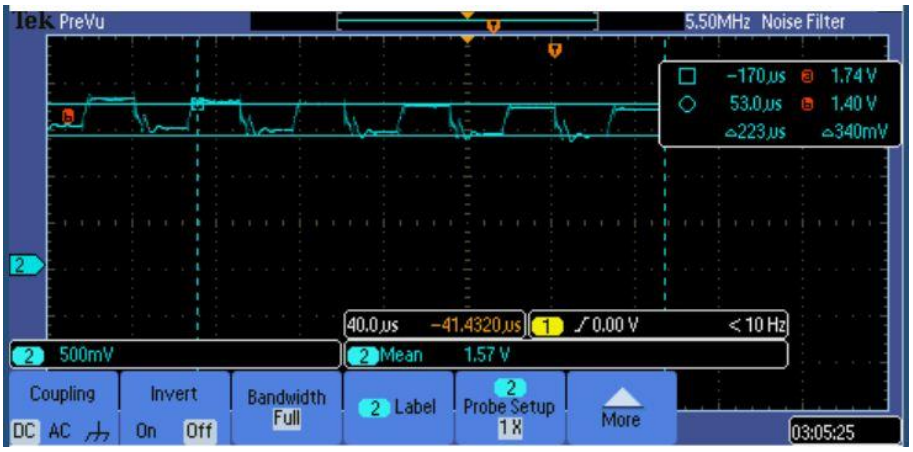

Figure 4.15. Voltage on flying capacitor C1 with cursors.

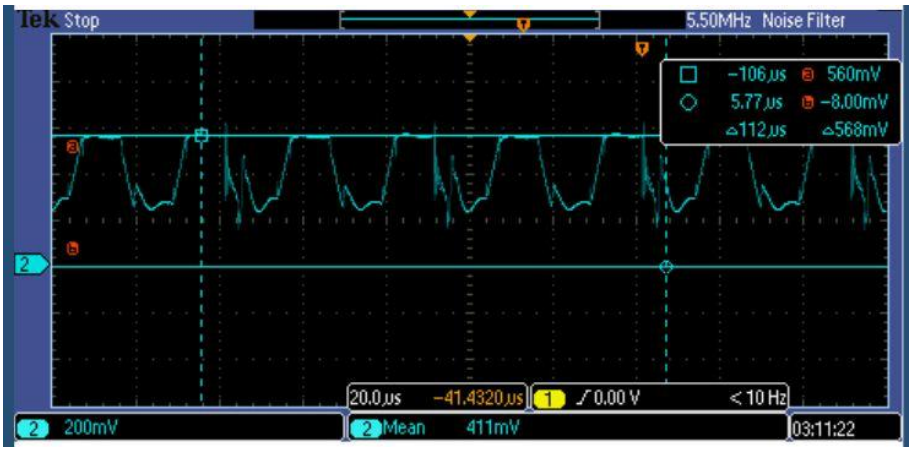

Figure 4.16. Voltage on flying capacitor C2 with cursors.

It can be noted that the ideal waveforms on the capacitors were achieved in the final two PCB implementations only, which proved to be one of the many requirements for correct operation, and consequently high efficiency.

4.1.3 Deadtime Waveforms

One of many techniques used to optimize performance in all converters is the addition of deadtime within the input signals to prevent overlapping caused by driver delays. As a result, a reduction of voltage spikes of over 50% is achieved, as is shown in Figures 4.17 and 4.18, for the *0.5-0.75Vin* operation region. Similarly, the same could be noticed in the *0.75-1Vin* operation region, as is shown in Figures 4.19 and 4.20.

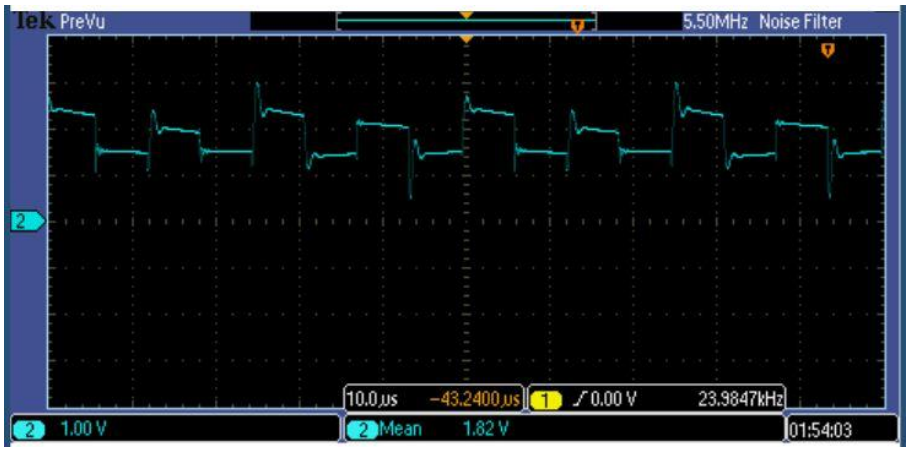

Figure 4.17. Voltage at the inductor (*Vx*) of the 5-Level hybrid operating at *0.5-0.75Vin* without deadtime.

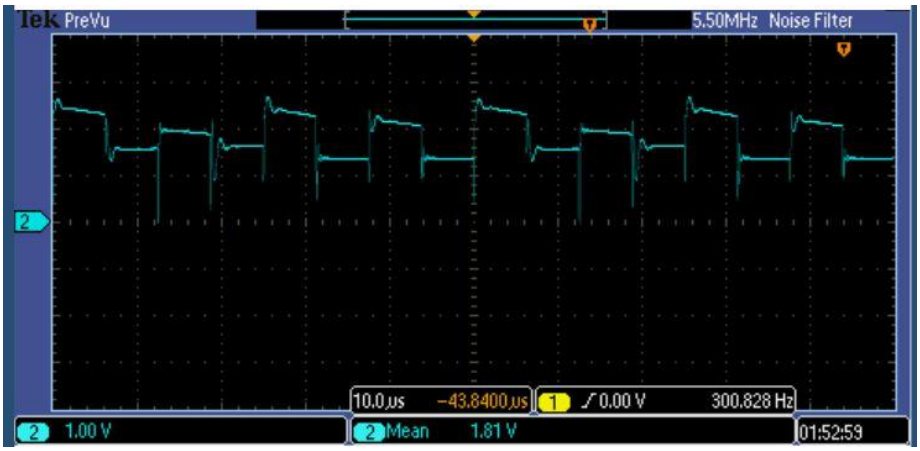

Figure 4.18. Voltage at the inductor (*Vx*) of the 5-Level hybrid operating at *0.5-0.75Vin* with deadtime.

Before implementing deadtime in the control signals, the maximum efficiency was affected by the high current spikes resulting from a momentary short circuit between the input voltage and ground. This can be noticed in the comparison between waveforms. The addition of deadtime eliminated the current spikes, but added a minute downward spike in output voltage, due to the momentary floating output. Adding excessive deadtime results in a more severe effect that is detrimental to overall efficiency, and could sometimes be more harmful than the control signals without deadtime. Accordingly, the deadtime is to be minimized and optimized for maximum efficiency.

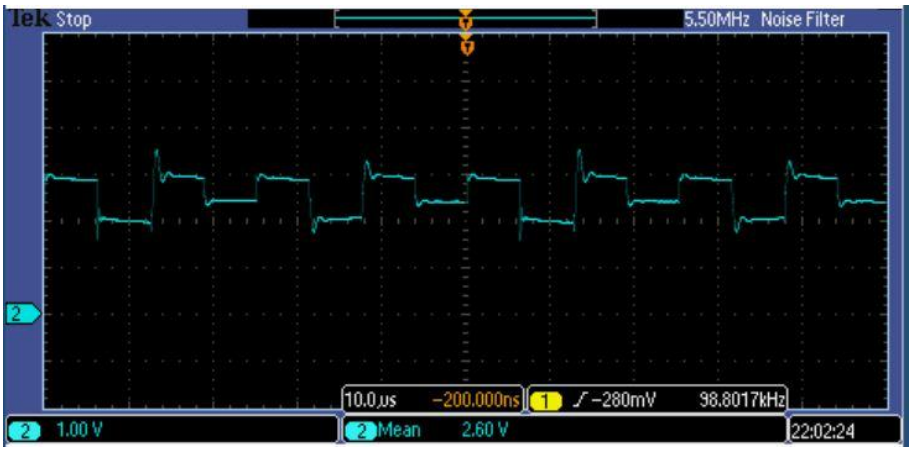

Figure 4.19. Voltage at the inductor (*Vx*) of the 5-Level hybrid operating at *0.75-1Vin* without deadtime.

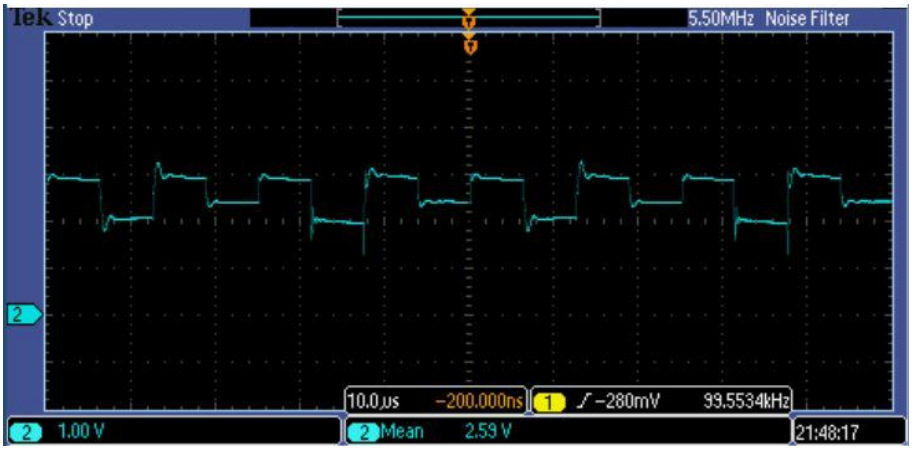

Figure 4.20. Voltage at the inductor (*Vx*) of the 5-Level hybrid operating at *0.75-1Vin* with deadtime.

4.2 Other Converter Implementations

4.2.1 Buck Converter Implementation Measurements

As for the testing of the Buck converter to be compared to the 5-Level Hybrid converter, it is clear from Figures 4.21, 4.22, and 4.23 that the voltage ripple at the inductor is four times higher than in the 5-Level, at different duty cycles.

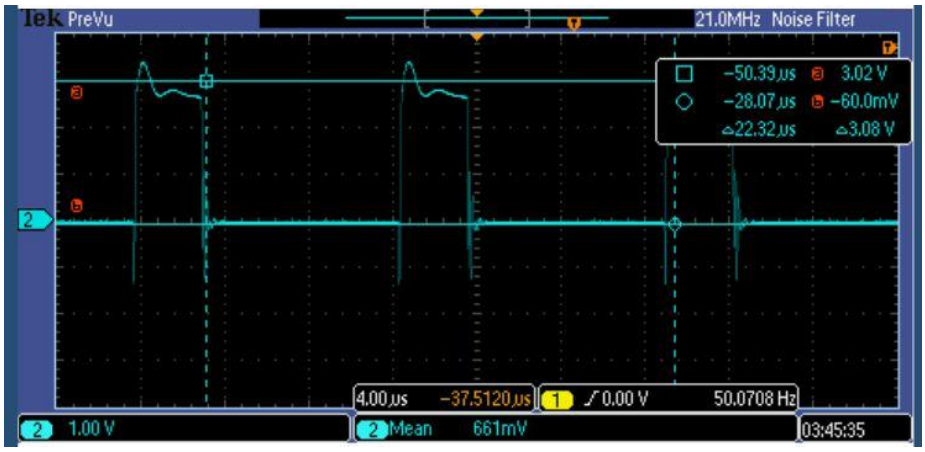

Figure 4.21. Voltage at the inductor (*Vx*) for a Buck converter with 25% duty cycle with cursors.

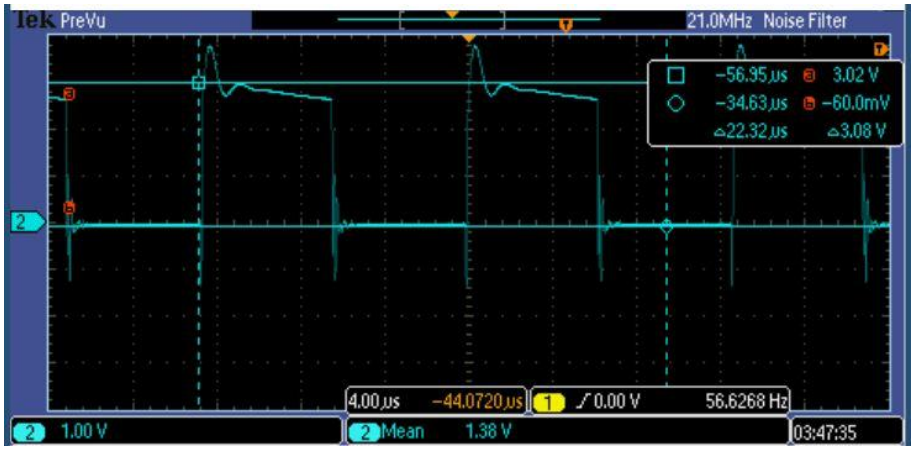

Figure 4.22. Voltage at the inductor (*Vx*) for a Buck converter with 50% duty cycle with cursors.

Unlike the 5-level hybrid, the traditional buck converter switches between two different levels which are *0* and *Vin*, which is four times higher when compared to the maximum ripple of *0.25Vin* found in the 5-level hybrid. At a 3V input voltage, the two buck converter levels are 0V and 3V, as demonstrated. This results in an output voltage of 1.38V at 50% duty cycle and increasing or decreasing the duty cycle produces a direct linear effect on the output voltage.

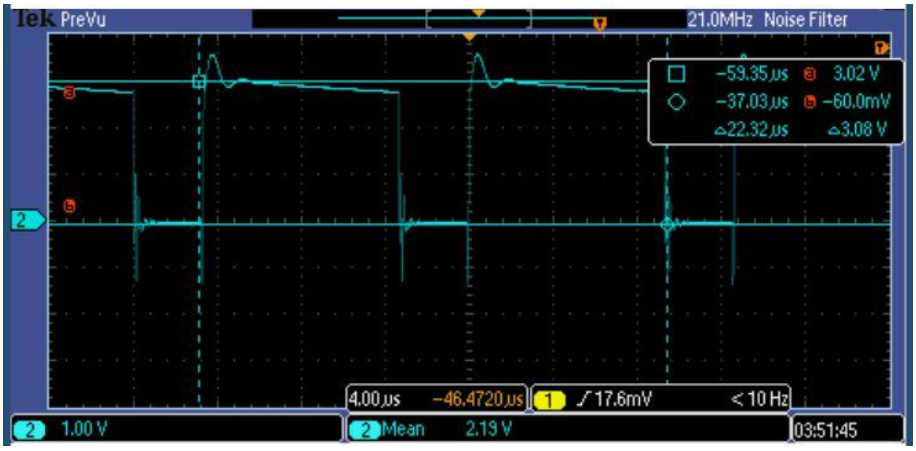

Figure 4.23. Voltage at the inductor (*Vx*) for a Buck converter with 75% duty cycle and cursors.

4.2.2 3-Level Hybrid Converter Implementation

The 3-Level Buck converter is also implemented using the same components and it also has twice as much voltage ripples than the 5-Level hybrid at the inductor. The 3-Level achieves a dynamic range of output voltages as well, according to the operation region and the duty cycle. Yet, the voltage ripple is twice as much, causing its efficiency to be less than that of the 5-Level hybrid. Despite correct functionality, the maximum efficiency achieved, which is demonstrated later, is less than the maximum efficiency obtained by the 5-Level hybrid throughout the range of conversion ratios.

4.2.2.1 3-Level Hybrid First Operation Region Waveforms

The voltage at the inductor (*Vx*) is measured in Figures 4.24, 4.25, and 4.26, at different duty cycles in the first operation region (0-0.5*Vin*) with *Vin*=3V, in which the levels are 0V and 1.5V. It is shown that correct functionality is achieved, and the performance compared to that of the 5-Level hybrid is discussed later in the chapter.

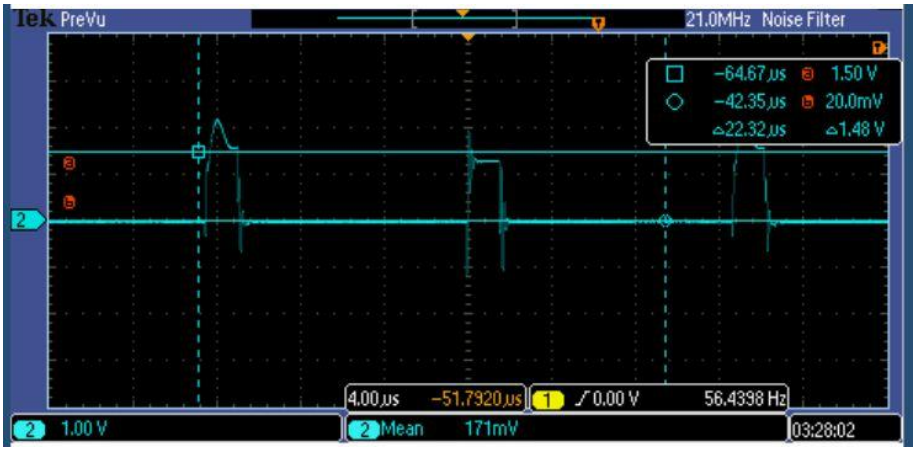

Figure 4.24. Voltage at the inductor of a test 3-Level converter in the first operation region at 25% duty cycle with cursors.

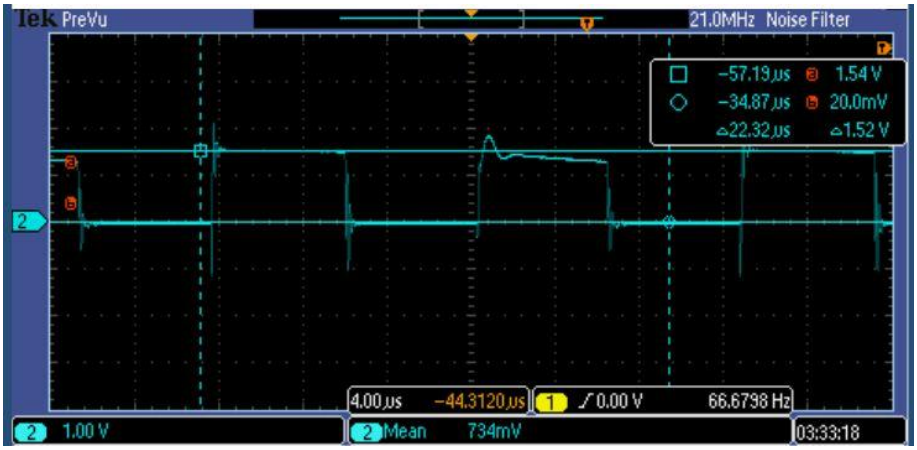

Figure 4.25. Voltage at the inductor of a test 3-Level converter in the first operation region at 50% duty cycle.

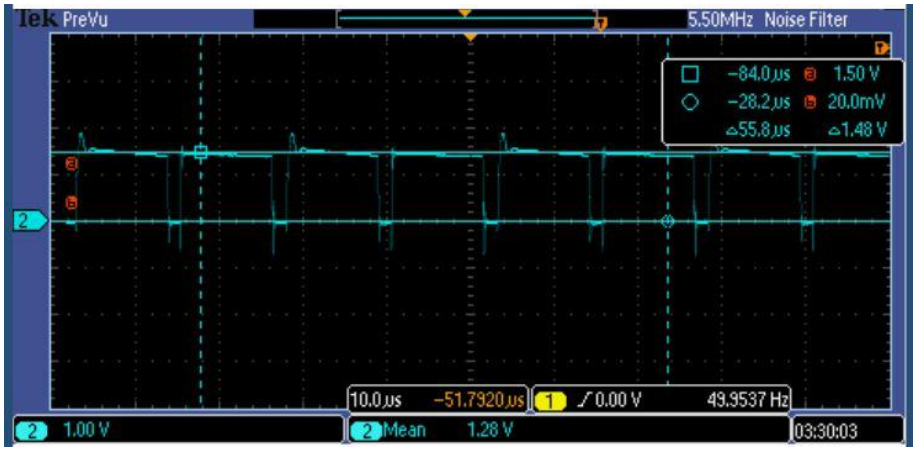

Figure 4.26. Voltage at the inductor of a test 3-Level converter in the first operation region at 75% duty cycle with cursors.

4.2.2.2 3-Level Hybrid Second Operation Region Waveforms

The same testing methodology was repeated and shown in Figures 4.27, 4.28, and 4.29 for the second operation region (0.5-1*Vin*) of the 3-Level hybrid, where the two levels being switched are 1.5V and 3V.

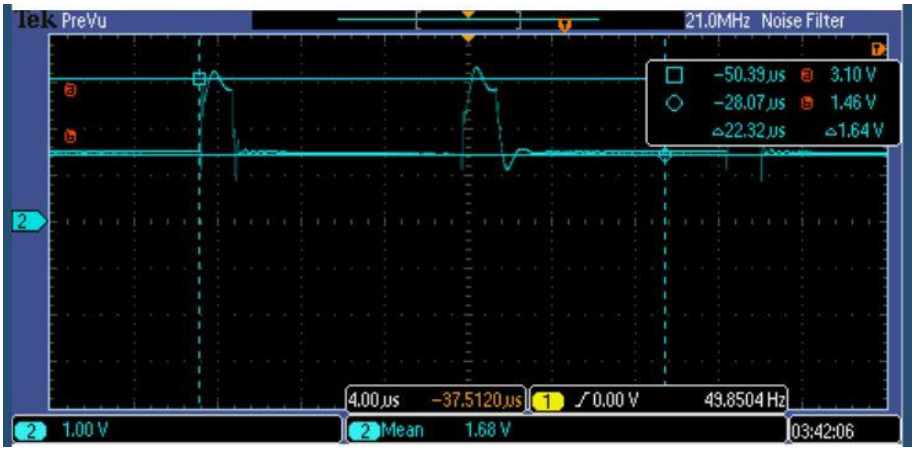

Figure 4.27. Voltage at the inductor of a test 3-Level converter in the second operation region at 25% duty cycle with cursors.

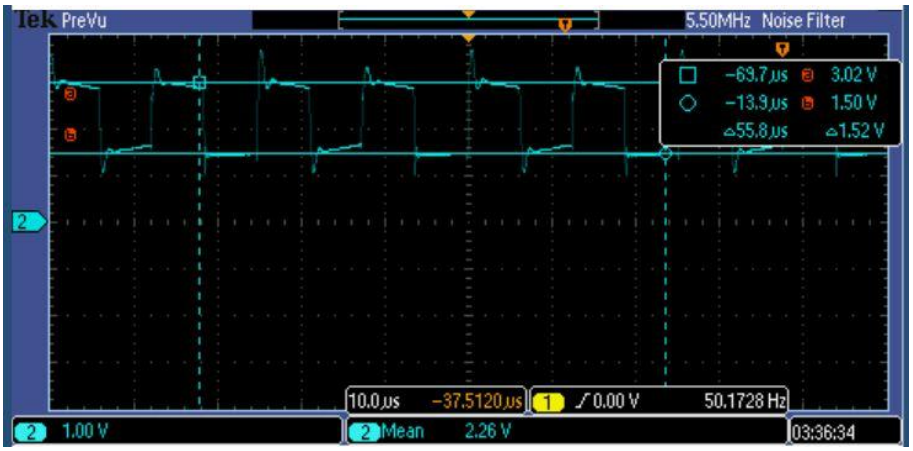

Figure 4.28. Voltage at the inductor of a test 3-Level converter in the second operation region at 50% duty cycle with cursors.

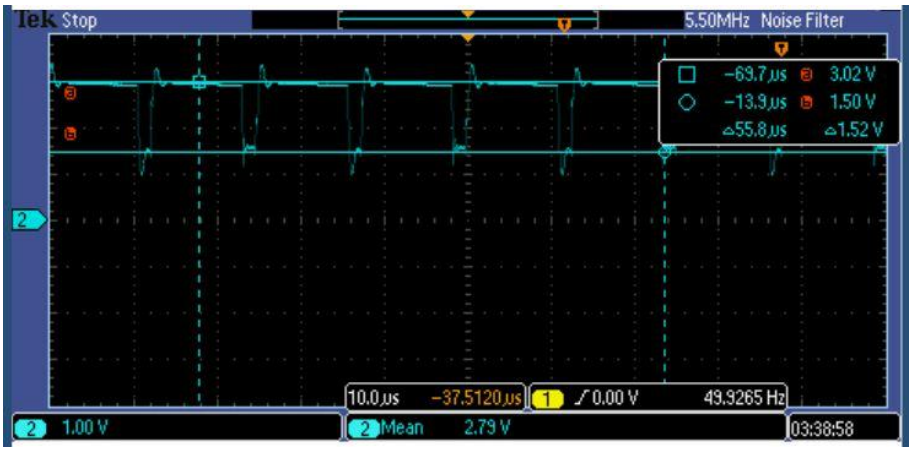

Figure 4.29. Voltage at the inductor of a test 3-Level converter in the second operation region at 75% duty cycle with cursors.

4.3 Output Voltage Ripples Measurements

As for the output voltage ripples, it is clear that the buck converter has much higher voltage ripples for the same components, frequency, and inductor size. This is displayed in Figure 4.30, where the conventional buck ripples exceed 50mV, while the 5-Level output ripples are less than 10mV, as is shown in Figures 4.31 and 4.32.

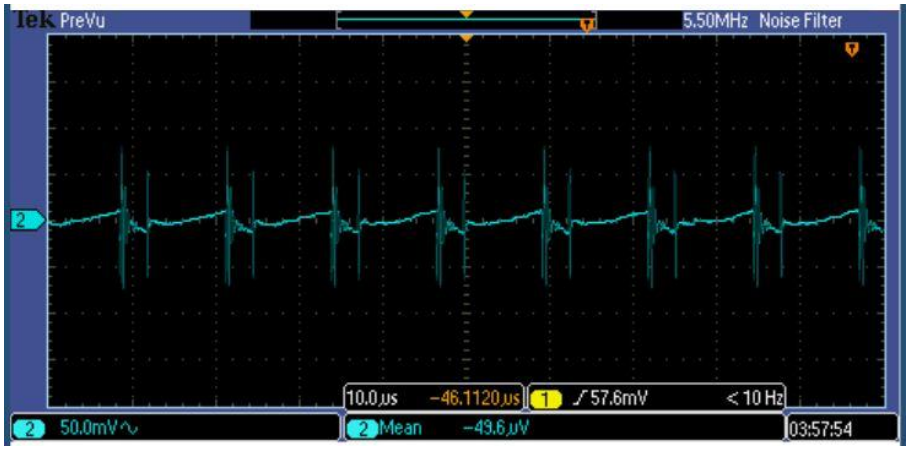

Figure 4.30. Conventional Buck output voltage ripples.

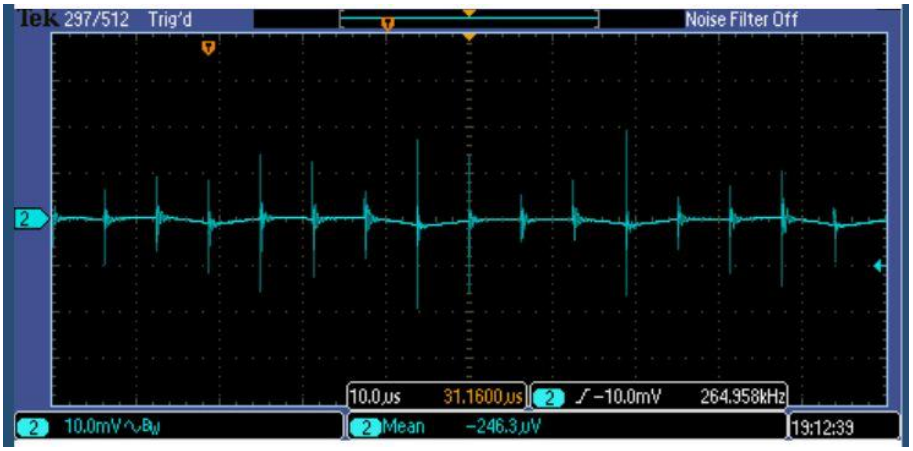

Figure 4.31. 5-Level Hybrid Buck output voltage ripples.

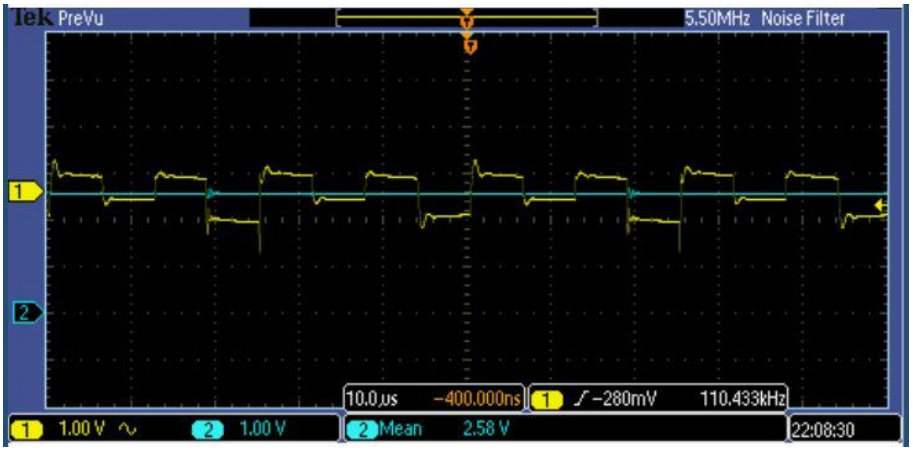

Figure 4.32. Voltage at the inductor (*Vx*) vs *Vout* for a 5-Level hybrid converter operating in the *0.75-1Vin* operation region.

It can be observed that the significant output voltage ripples in the buck converter are caused by the switching, where the high voltage difference at the inductor, which is equal to the input voltage, produces a noticeable effect in the output. However, for the 5-Level converter, the voltage difference at the inductor is one quarter of the input voltage, and therefore does not negatively affect the output voltage ripples, and produces a smooth DC signal. This is an appealing feature in the 5-Level hybrid which proves its distinction over the buck converter under the same testing conditions, and using identical components.

4.4 Performance Comparison between Converters

As for performance, it can be seen from Figure 4.33 that all conversion ratios are achieved at an input voltage of 3V, and that the same was done for 5V. At different load resistances, several efficiency curves can be obtained, demonstrating the optimum load for the converter.

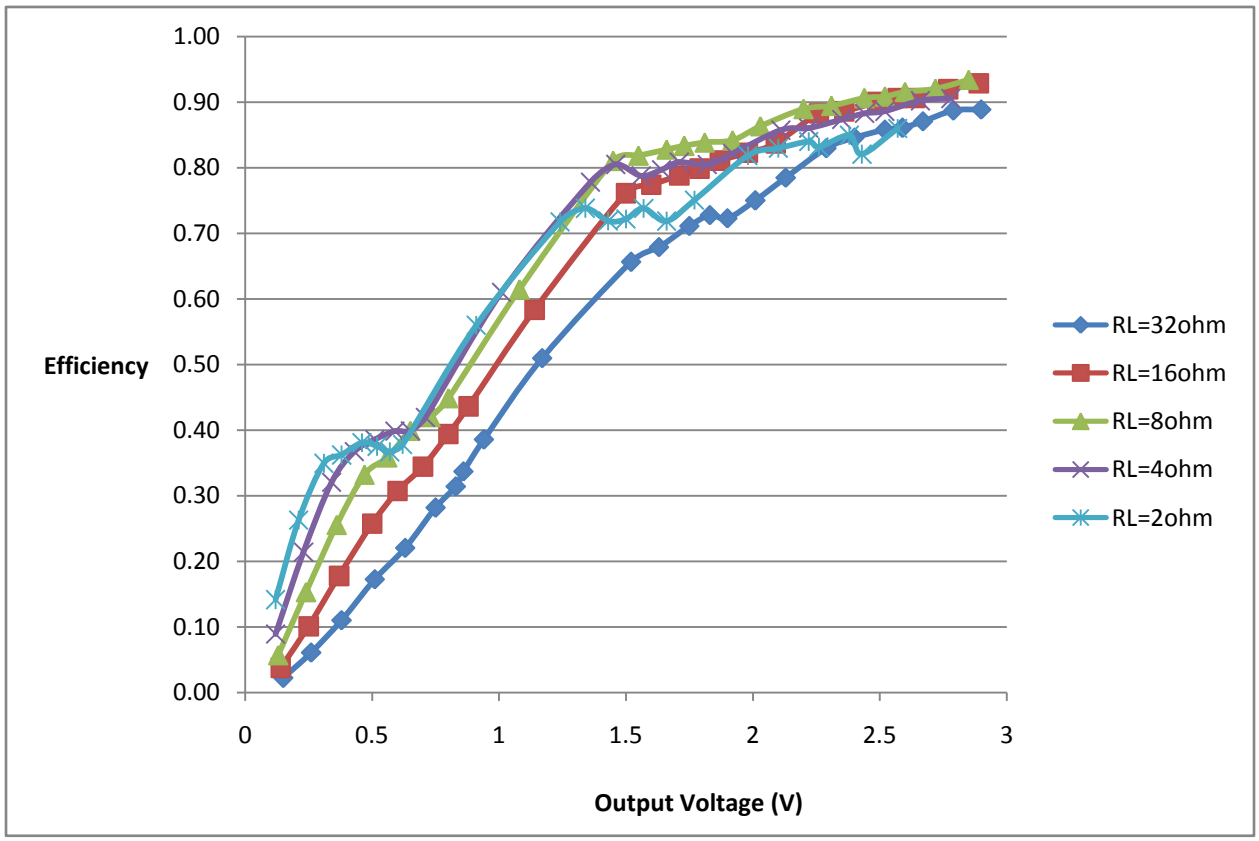

Figure 4.33. Efficiency vs. Output voltage (V) of the 5-Level Hybrid at multiple load resistances (Ω) witb *Vin*=3V.

It is also shown in Figure 4.34 that several output voltages result in a shift in the efficiency curves with respect to load current. The higher conversion ratios at a 3V input are clearly superior in their efficiency. Yet, reasonably good performance (efficiency is maintained above 80%) can be obtained at output voltages between 1.5V to 2.9V, at medium load currents.

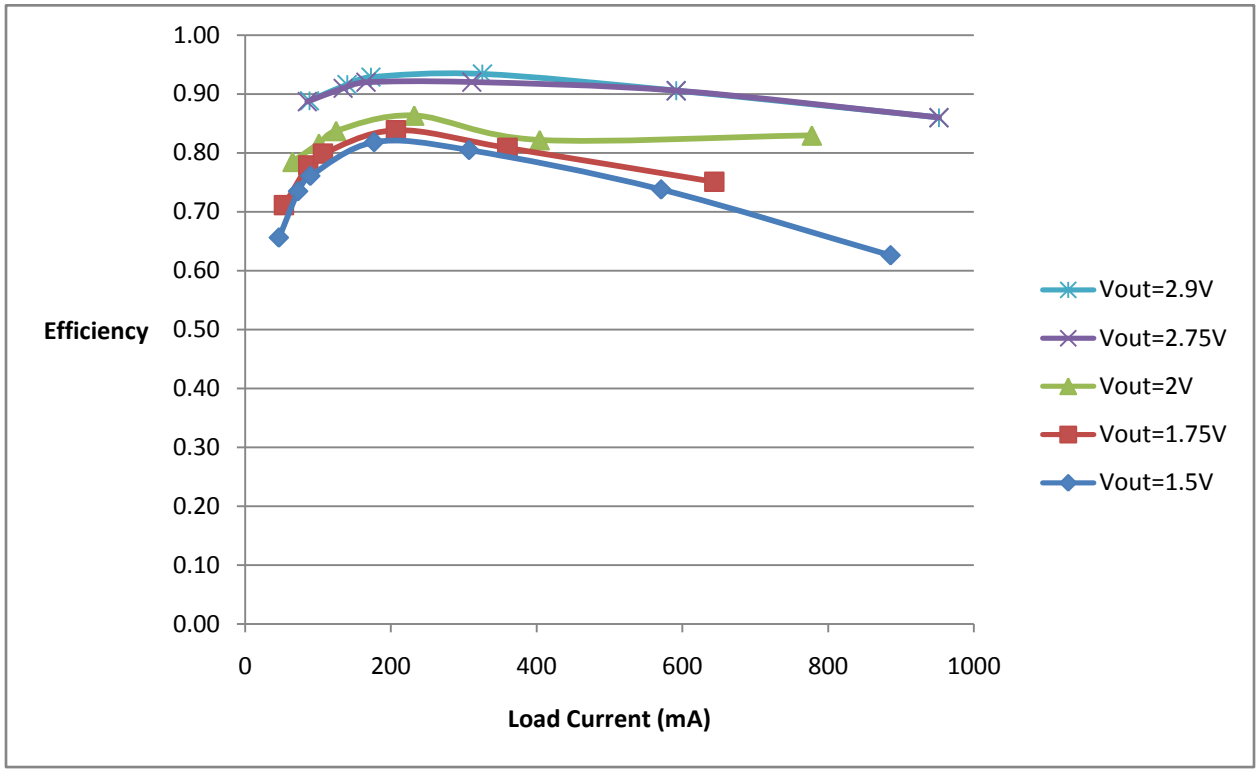

Figure 4.34. Efficiency vs. Load Current (mA) of the 5-Level hybrid converter at multiple output voltages (V).

However, it is essential to compare the performance between the 5-Level Hybrid Converter, the 3-Level Buck Converter, and the traditional Buck Converter. According to the results, the 5-Level Hybrid exceeds the 3-Level and the Buck converters in low load currents, and all three converters tend to behave similarly under high load currents. In Figure 4.35 as well as Figure 4.36, it is clear that for load currents between 100mA and 500mA, the 5-Level converter is optimized using this inductance and switching frequency. However, for increased load currents, the 5-Level behaves like a traditional Buck converter when it comes to efficiency, despite its improved output voltage ripples.

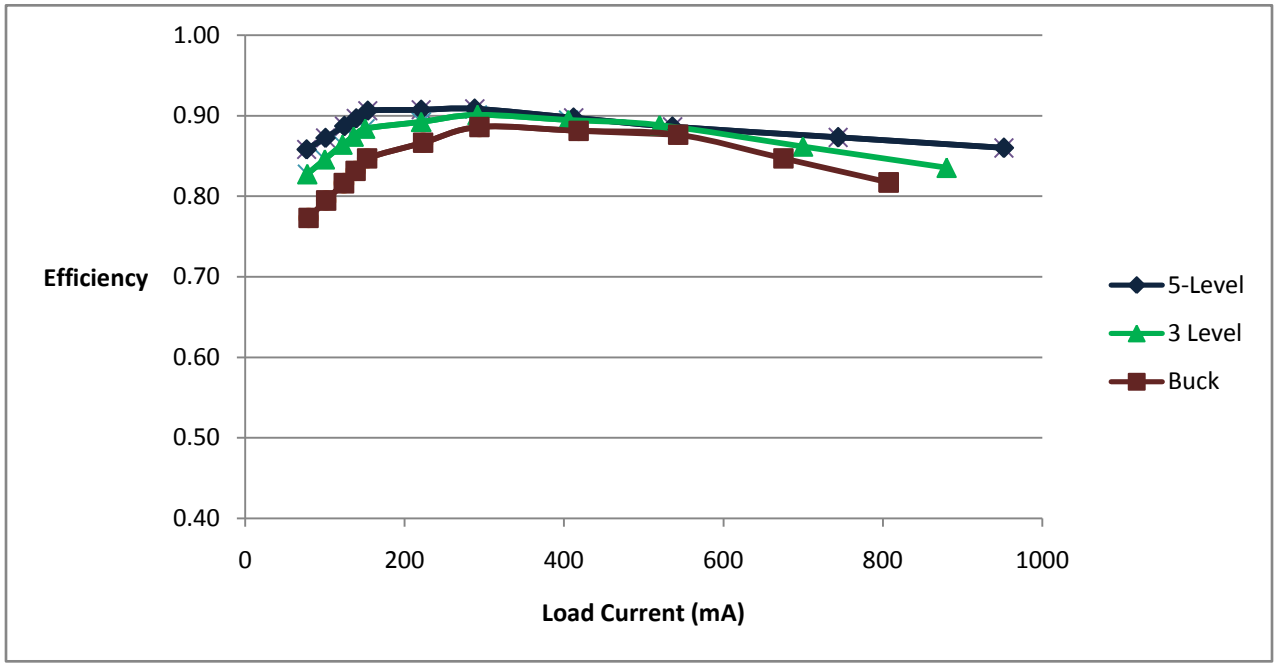

Figure 4.35. Efficiency vs. Load Current (mA) of the three converter types at *Vout*=2.5V with *Vin*=3V.

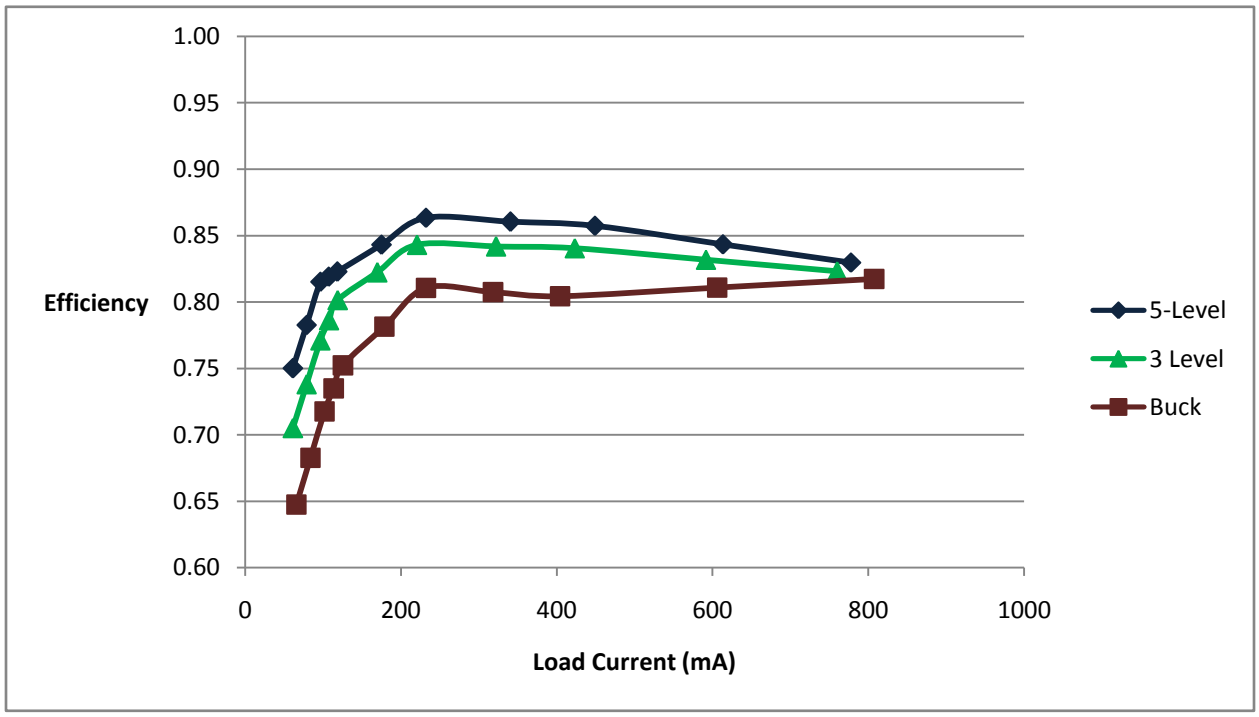

Figure 4.36. Efficiency vs. Load Current (mA) of the three converter types at *Vout*=2V with *Vin* =3V.

At a 32Ω load resistance, which consumes relatively small load currents, the 5-Level is shown in Figure 4.37 to improve on the 3-Level Buck and the traditional Buck Converters by 5-15% depending on the output voltage and conversion ratio, using the same phase frequency of 160kHz and inductance of 50uH. Therefore, it is clear that the 5-Level provides higher performance than a traditional Buck at specific operating points.

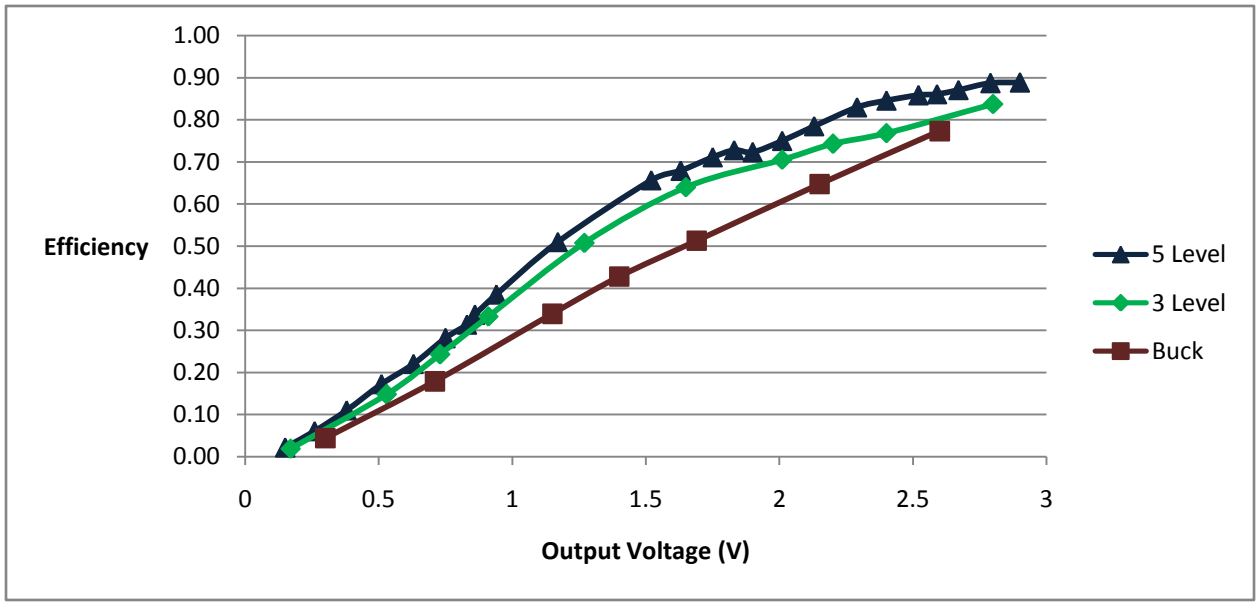

Figure 4.37. Efficiency vs. Output Voltage (V) of the three converter types at a Load resistance of 32Ω.

4.5 Chapter Summary

To sum up, the measured waveforms at the inductor input (*Vx*) prove correct operation of the hybrid 5-Level DC-DC converter, which was implemented with limitations on the components. The 3-Level hybrid and the traditional buck converters were also implemented under identical conditions to compare and contrast the performance and output waveform characteristics, and were measured to ensure correct functionality. The measured performance proves an advantage of the 5-Level topology over other converters in terms of conversion and overall efficiency, despite including the switching losses, which are higher for this topology due to increased overhead circuitry. Nevertheless, the 5-Level converter proved its domination in efficiency over a wide range of output voltages and output load currents.

Chapter 5

CONCLUSION AND FUTURE WORK

5.1 Conclusion

Mobile, battery powered devices have also become a large segment of the electronics industry, providing a major source of motivation for DC-DC converter improvements. Consumer electronics are improving in performance with the development of new technologies and consume more power, which is accompanied by a reduction in their size. Therefore, it is necessary to keep up with the trend from a power electronics perspective, by developing more advanced power supply units, which are more efficient, and smaller in size.

In this work, a hybrid voltage regulator topology is evaluated, implemented, and compared using experimental measurements. The hybrid topology addresses the limitations of the two dominant VR types by combining elements of both types. These limitations include integrability and performance when there are restrictions on component size and operating conditions.

A 5-Level Hybrid converter is designed and implemented using elements from SCVRs and from the traditional Buck converter. The hybrid switches between any two of the five possible levels, which the inductor filters in order to produce an output between the two levels, according to the duty cycle. This topology presents a compromise between the advantages of both traditional converter types, as is shown in Table 5.1.

Table 5.1. Performance Comparison between Traditional Converters and the 5-Level Hybrid

Criterion	**SCVRs**	**Buck**	**5-Level Hybrid**
Maximum Efficiency	Limited	High	High
Area Requirements	Low	High	Medium
Integrability	Simple	Complex	Average
Control Overhead	High	Low	High
Output Voltage Ripples	Low	High	Low

The PCB implementations were designed for ideal functionality and high efficiency, by selecting the optimal components and operating conditions. The components include the switches, capacitors, inductor, and MOSFET drivers, while the operating conditions include the operating voltages, switching frequency, and load currents. The operating conditions are based on the average requirements for mobile, laptop, and tablet devices, where a high power DC-DC converter is desired with minimalistic area requirements.

The 5-Level converter has been proven to increase efficiency at low load currents by decreasing the voltage ripple, and has decreased the output ripples significantly when compared to the traditional buck converter and other works including the 3-Level Buck converter. The advantages are mainly demonstrated in a specific operating point, when there are restrictions on the output ripples, inductor size, quality factor, total PCB area, and switching frequency.

5.2 Future Work

Future work may include several novel or existing improvements to the hybrid DC-DC converter topology. Further improvements can be targeting increased efficiency or decreased converter area, which would allow simpler integrability.

It would be beneficial to follow-up with implementations of more topologies utilizing the same or a different concept, while remaining within the hybrid VR framework. This is essential

to evaluate the different hybrid structures, which will inevitably become the dominant trend in voltage regulators.

For future implementations, further integrability is targeted with more advanced controllers which lead to higher overall efficiency. The microcontroller used in the implementations in this work could be integrated on a double-sided PCB with this converter. Another concept would be to utilize an 8-bit microcontroller with a more compact footprint for integration on the same PCB side.

Another controller considered for the hybrid 5-Level converter implementation would be a Field-Programmable-Gate-Array (FPGA), which would provide more accurate control signals, as well as the potential to add a feedback mechanism. The feedback mechanism was attempted with the microcontroller and resulted in decreased efficiency due to inconsistent control signals. Therefore, an FPGA would allow two applications to run simultaneously: the control signals and the feedback loop. The feedback loop would include a reference voltage to follow and a regulation program to maintain the output voltage with changes to load current.

Other control mechanisms are also considered, such as digital capacitance modulation, which can be an alternative or additional control mechanism, as it is very promising. Digital capacitance modulation provides an efficient method to maintain regulation against load current changes [16]. This technique preserves a constant frequency while scaling switching losses with changes in load current. Therefore, high efficiency can be achieved across different load current levels while maintaining a predictable switching noise behavior.

Hybrid DC-DC converters are found to be a wide and promising area of research. Consequently, exploring more advanced DC-DC converter control mechanisms and components is the track to obtain higher efficiency for the current design. Furthermore, expanding on the existing hybrid design and using other topologies is also promising for obtaining better performance and more compact layouts.

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